

8

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1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MLB, M1

01/06/2006

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD
DATE

ENG APPD
DATE

A

41882

PRODUCTION RELEASED

01/06/06

06

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N/A

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N/A

N/A

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Functional / ICT Test

N/A

N/A

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Signal Aliases

N/A

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M42

11/16/2005

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(MASTER)

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10/07/2005

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10/12/2005

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SCHEMATIC / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6941	1	SCHEM,MLB,M1	SCH	CRITICAL	
820-1881	1	PCBF,MLB,M1	PCB	CRITICAL	

DRAWING
TITLE=M1_MLB
ABBRV=DRAWING
LAST_MODIFIED=Fri Jan 6 18:57:50 2006

DIMENSIONS ARE IN MILLIMETERS

XX ± _____

X.XX ± _____

X.XXX ± _____

ANGLES ± _____

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER	/	DESIGN CK	/
ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	NONE
MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER 051-6941
		REV. A	SHT 1 OF 104

Apple Computer Inc.

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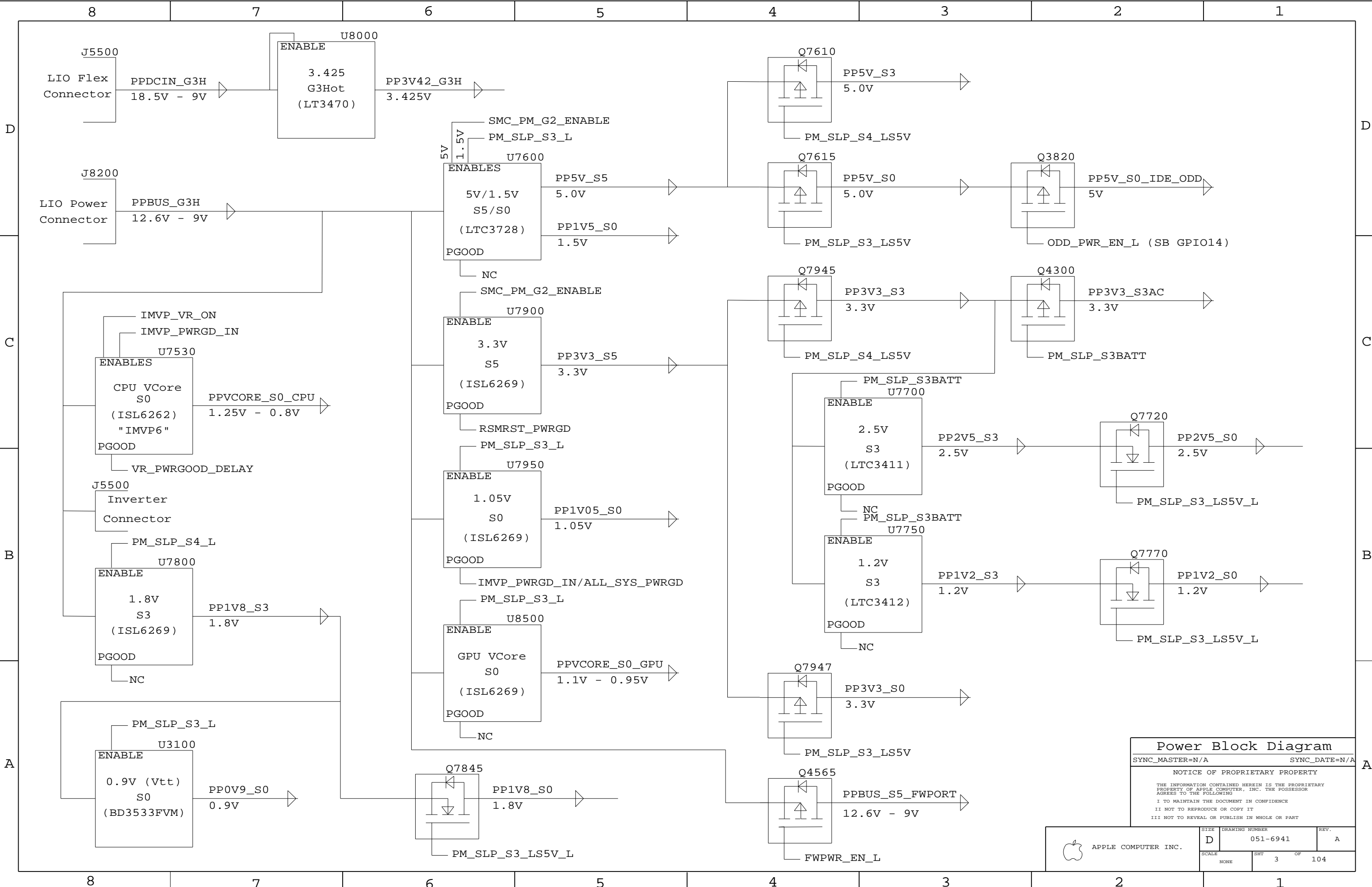
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SCHEM,MLB,M1



Power Block Diagram

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SYNC_DATE=N/A

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"Better" BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7403	PCBA,MLB_BTR,SAM128,M1	EEE_UNK,M1_COMMON,CPU_BTR,VRAM_SAM128

630-7401 is placeholder for PCBA,MLB_BTR,HY128,M1 (EEE:UNH)

"Best " BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7254	PCBA,MLB_BST,SAM256,M1	EEE_TYY,M1_COMMON,CPU_BST,VRAM_SAM256

630-7402 is placeholder for PCBA,MLB_BST,HY256,M1 (EEE:UNJ)

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M1_COMMON	COMMON,M1_COMMON1,M1_COMMON2,M1_COMMON3
M1_COMMON1	BOOTROM_FINAL,ENET_LOM_DISABLE,ENETPWR_S3AC,GPU_BB_CTL,GPUTHM_A_GPU,HSTHMSNS_HAS
M1_COMMON2	ITP,INVERTER_BUF,KBDLED_HAS,LPCPLUS,LVDS_PD,MEMVREF_S3,MEMVTT_EN_PU
M1_COMMON3	RTUSB_ESD,SMC_PRGRM,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
VRAM_HY128	GPU_MEM_HYNIX,VRAM_128_HYNIX
VRAM_SAM128	VRAM_128_SAMSUNG
VRAM_HY256	GPU_MEM_256M,GPU_MEM_HYNIX,VRAM_256_HYNIX
VRAM_SAM256	GPU_MEM_256M,VRAM_256_SAMSUNG

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TYY]	CRITICAL	EEE_TYY	M1,BST,SAM256
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNH]	CRITICAL	EEE_UNH	M1,BTR,HY128 (UNUSED)
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNJ]	CRITICAL	EEE_UNJ	M1,BST,HY256 (UNUSED)
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNK]	CRITICAL	EEE_UNK	M1,BTR,SAM128

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
337S3267	1	IC,M1 BTR,479 BGA	U0700	CRITICAL	CPU_BTR
337S3268	1	IC,M1 BST,479 BGA	U0700	CRITICAL	CPU_BST
341S1812	1	IC,EFI,BOOTROM DEVELOPMENT,M1	U6301	CRITICAL	BOOTROM_DEVEL
341S1813	1	IC,EFI,BOOTROM FINAL,M1	U6301	CRITICAL	BOOTROM_FINAL
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1843	1	IC,PRGRM,SMC,M1	U5800	CRITICAL	SMC_PRGRM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	CRITICAL	
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0309	1	IC,ATI,M56P,GRPSCCTRL,880BGA,LF	U8400	CRITICAL	
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,S08	U4102	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
353S1235	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	
359S0101	1	IC,CY28445~5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	

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BOM Configuration

SYNC_MASTER=N/A

SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-6941

REV.

A

SCALE

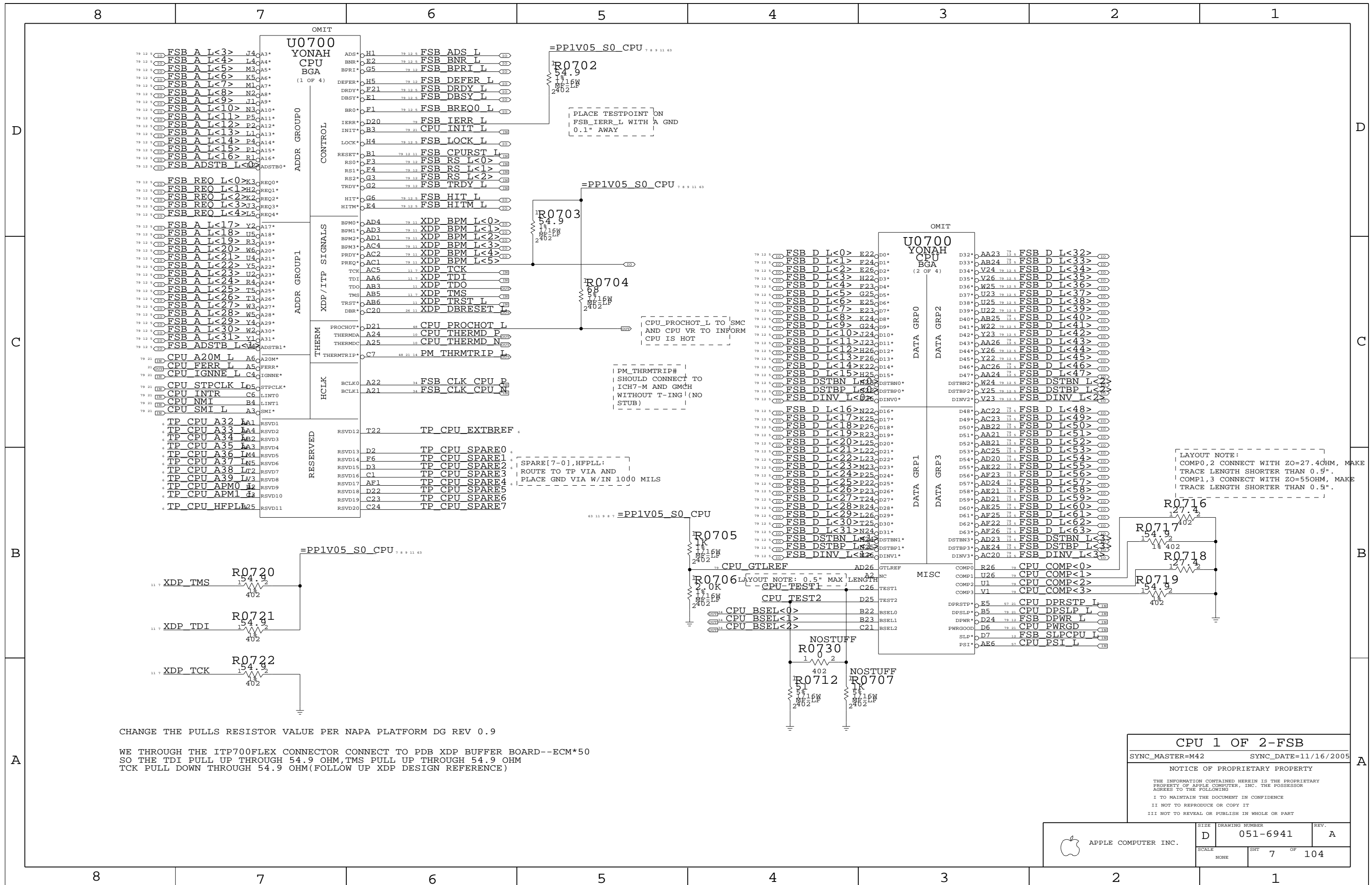
NONE

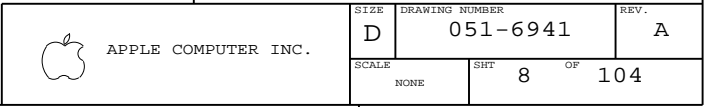
SHT

4

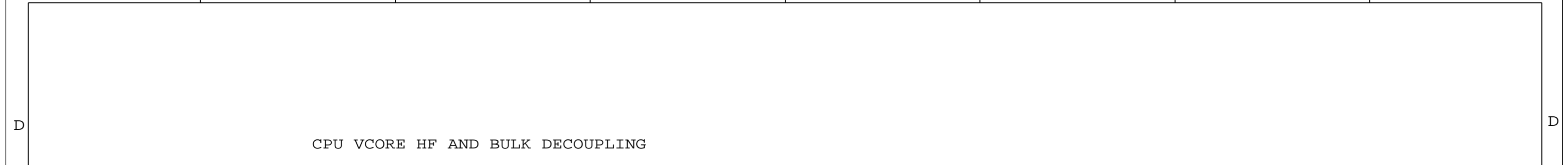
OF

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4x 470uF. 20x 22uF 0805

1 C0900 22uF 20% 6.3V X5R 0805

1 C0901 22uF 20% 6.3V X5R 0805

1 C0902 22uF 20% 6.3V X5R 0805

1 C0903 22uF 20% 6.3V X5R 0805

1 C0904 22uF 20% 6.3V X5R 0805

1 C0905 22uF 20% 6.3V X5R 0805

1 C0906 22uF 20% 6.3V X5R 0805

1 C0907 22uF 20% 6.3V X5R 0805

1 C0908 22uF 20% 6.3V X5R 0805

1 C0909 22uF 20% 6.3V X5R 0805

1 C0910 22uF 20% 6.3V X5R 0805

1 C0911 22uF 20% 6.3V X5R 0805

1 C0912 22uF 20% 6.3V X5R 0805

1 C0913 22uF 20% 6.3V X5R 0805

1 C0914 22uF 20% 6.3V X5R 0805

1 C0915 22uF 20% 6.3V X5R 0805

1 C0916 22uF 20% 6.3V X5R 0805

1 C0917 22uF 20% 6.3V X5R 0805

1 C0918 22uF 20% 6.3V X5R 0805

1 C0919 22uF 20% 6.3V X5R 0805

CRITICAL 1 C0950 470uF-7MOHM 20% 2.5V TANT D2T

CRITICAL 1 C0952 470uF-7MOHM 20% 2.5V TANT D2T

CRITICAL 1 C0953 470uF-7MOHM 20% 2.5V TANT D2T

CRITICAL 1 C0954 470uF-7MOHM 20% 2.5V TANT D2T

CPU VID<0> CPU VID<1> CPU VID<2> CPU VID<3> CPU VID<4> CPU VID<5> CPU VID<6>

IMVP6 VID<0> IMVP6 VID<1> IMVP6 VID<2> IMVP6 VID<3> IMVP6 VID<4> IMVP6 VID<5> IMVP6 VID<6>



VCCP (CPU I/O) Decoupling

1x 470uF, 6x 0.1uF 0402

C0935 470uF-7MOHM

C0936 0.1uF

C0937 0.1uF

C0938 0.1uF

C0939 0.1uF


C0940 0.1uF

C0941 0.1uF

NOTE: This cap is shared between CPU and NB

GND



 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	A
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	NONE	9	104

LAYOUT NOTE:
ADD GND GUARD TRACE
FOR CPU_THERMD_P AND
CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND
CPU_THERMD_N ON SAME
LAYER.
10 MIL TRACE
10 MIL SPACING

PLACEHOLDER ADT7461A

CRITICAL1

U1001
ADT7461


THRM_ALERT L
THRM_ALERT

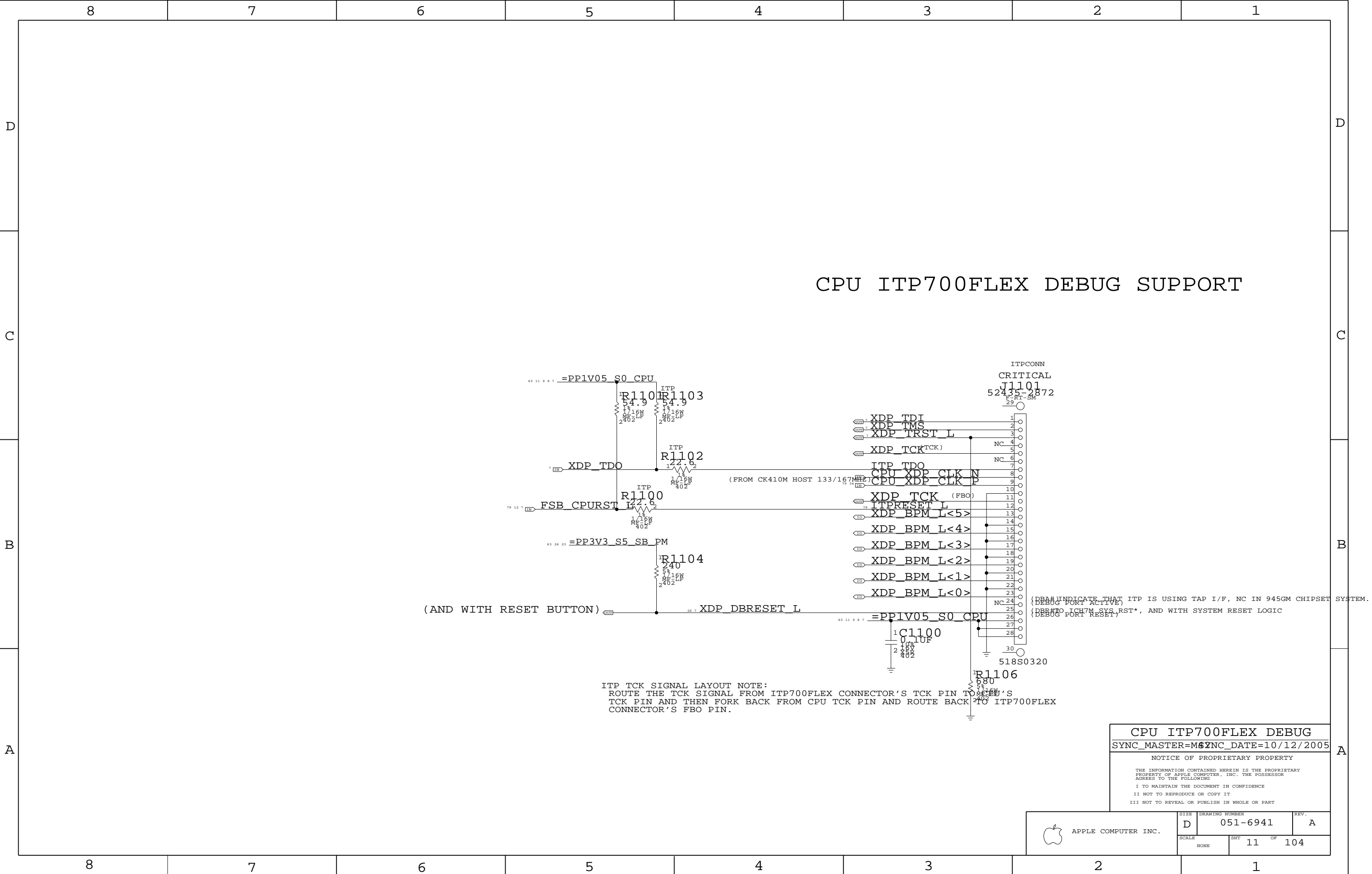
SMB_THRM_CLK
SMB_THRM_DATA

PLACE U1001 NEAR THE U1200

PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR	
SYNC_MASTER=M42	SYNC_DATE=10/07/2005
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D

C

B

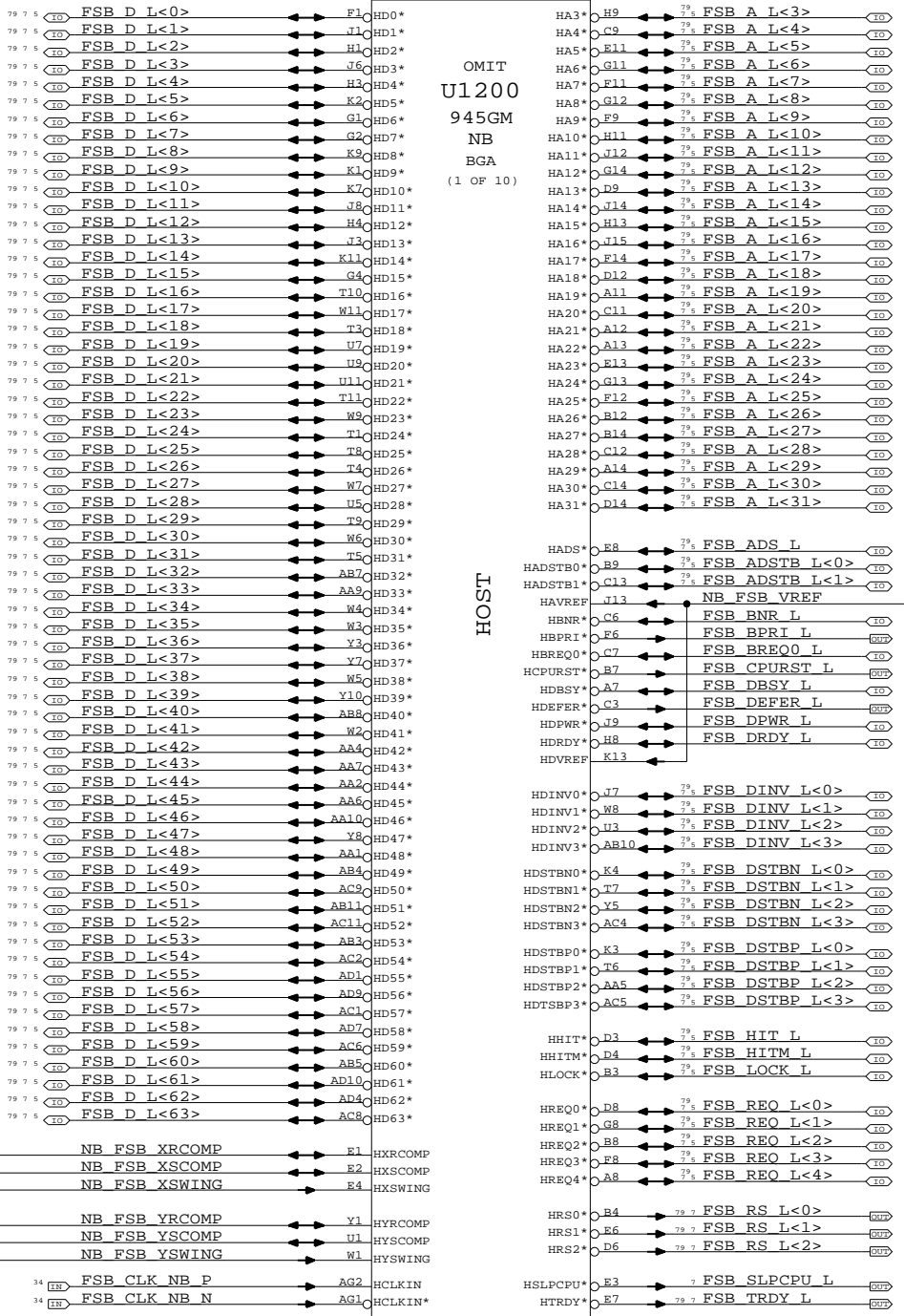
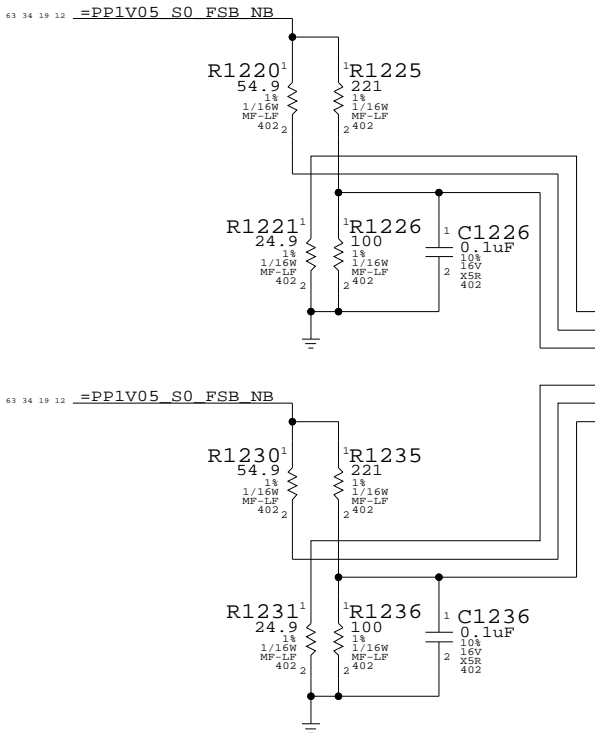
A

D

C

B

A



NB CPU Interface

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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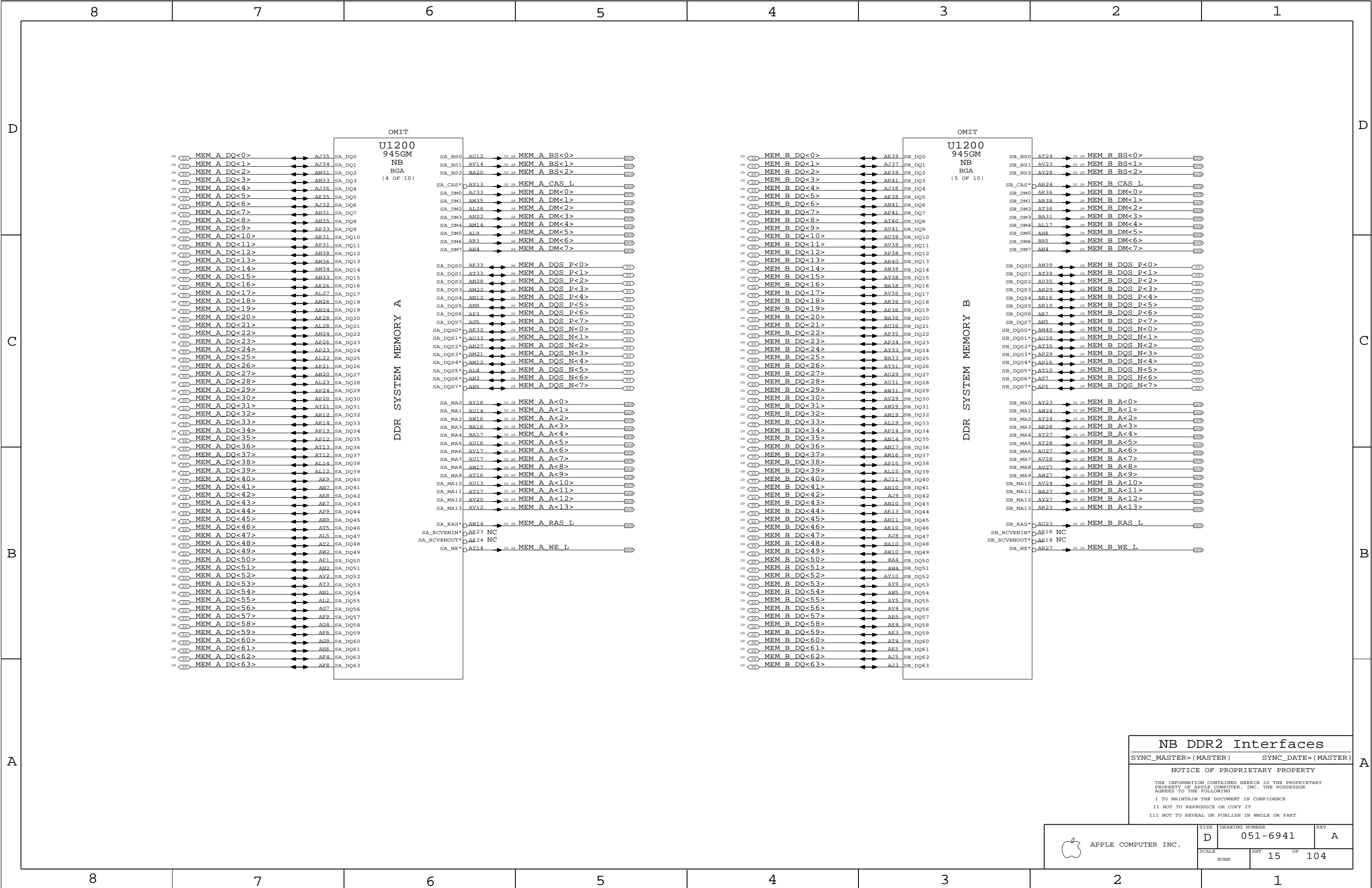
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NONE			



NB DDR2 Interfaces

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

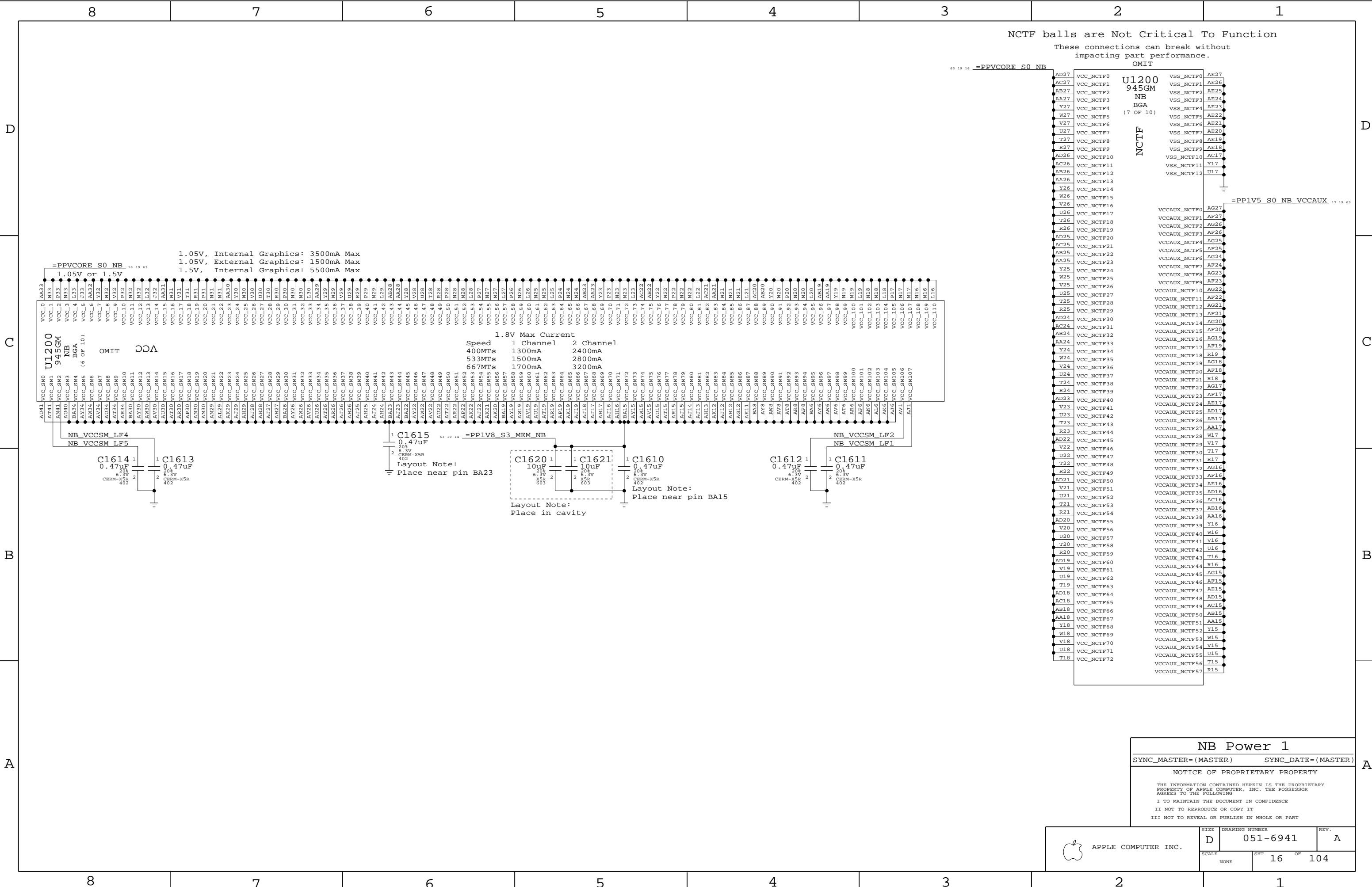
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NB Power 1

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

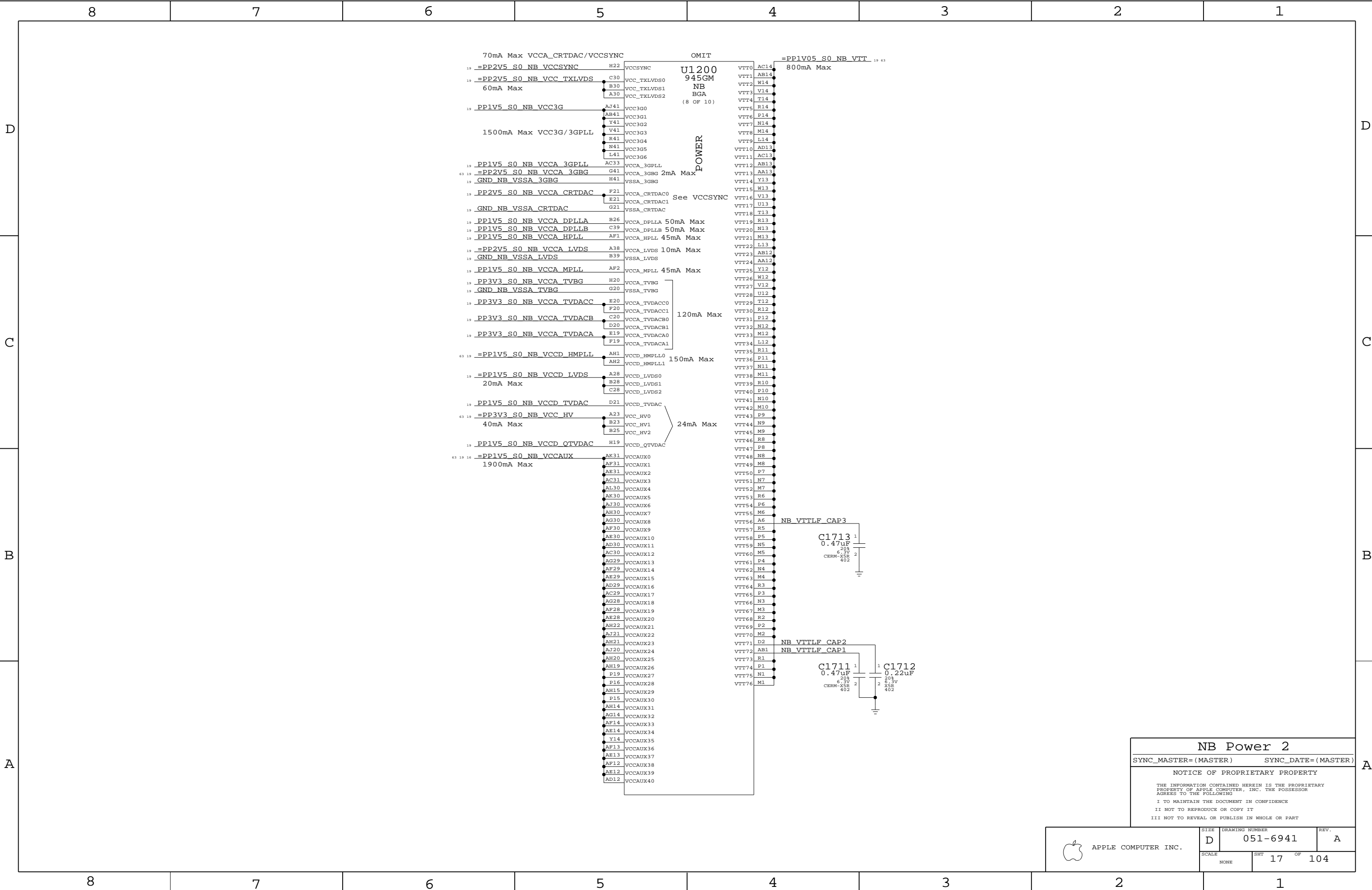
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NB Power 2

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

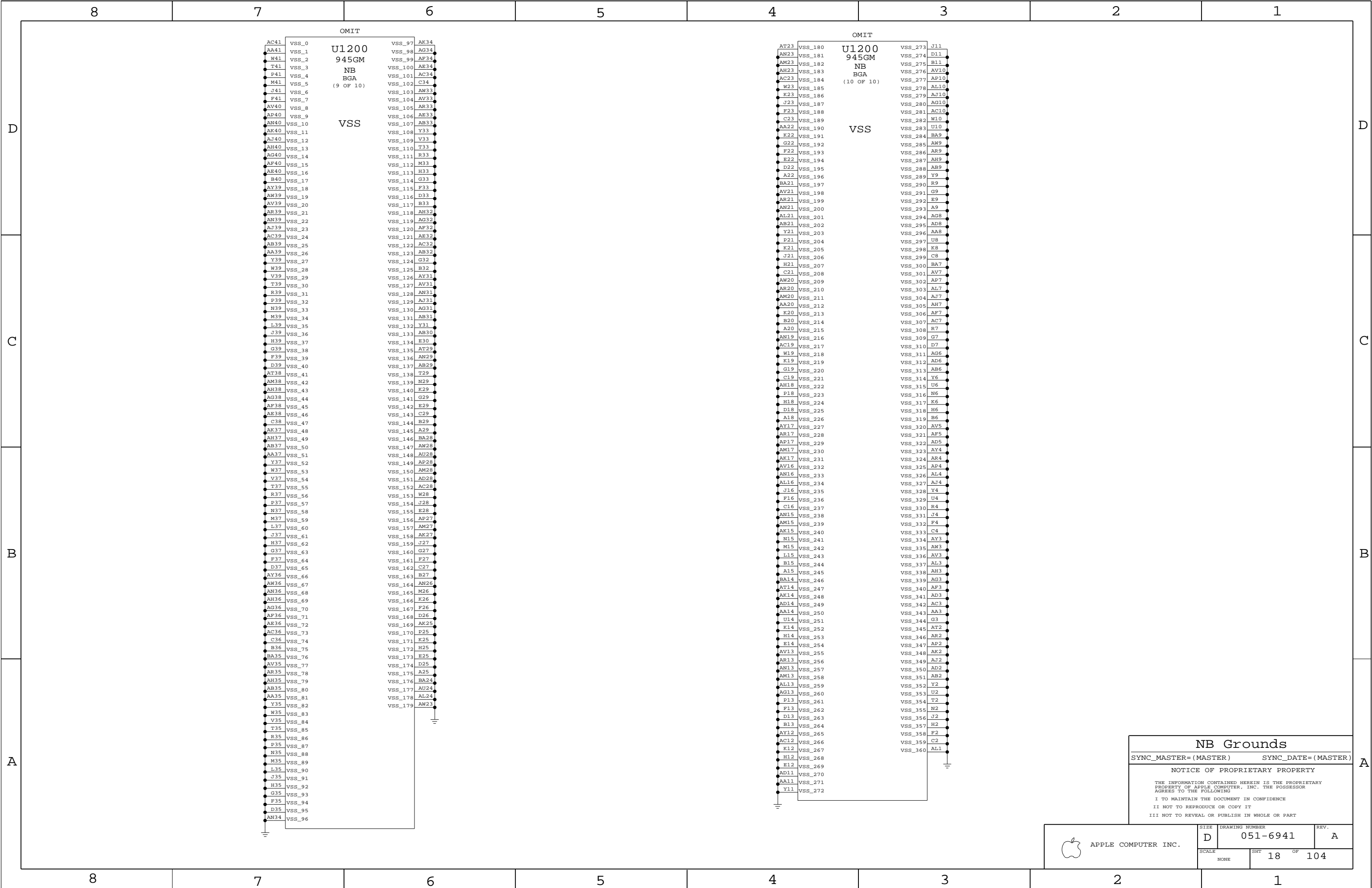
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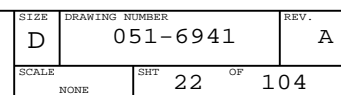
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

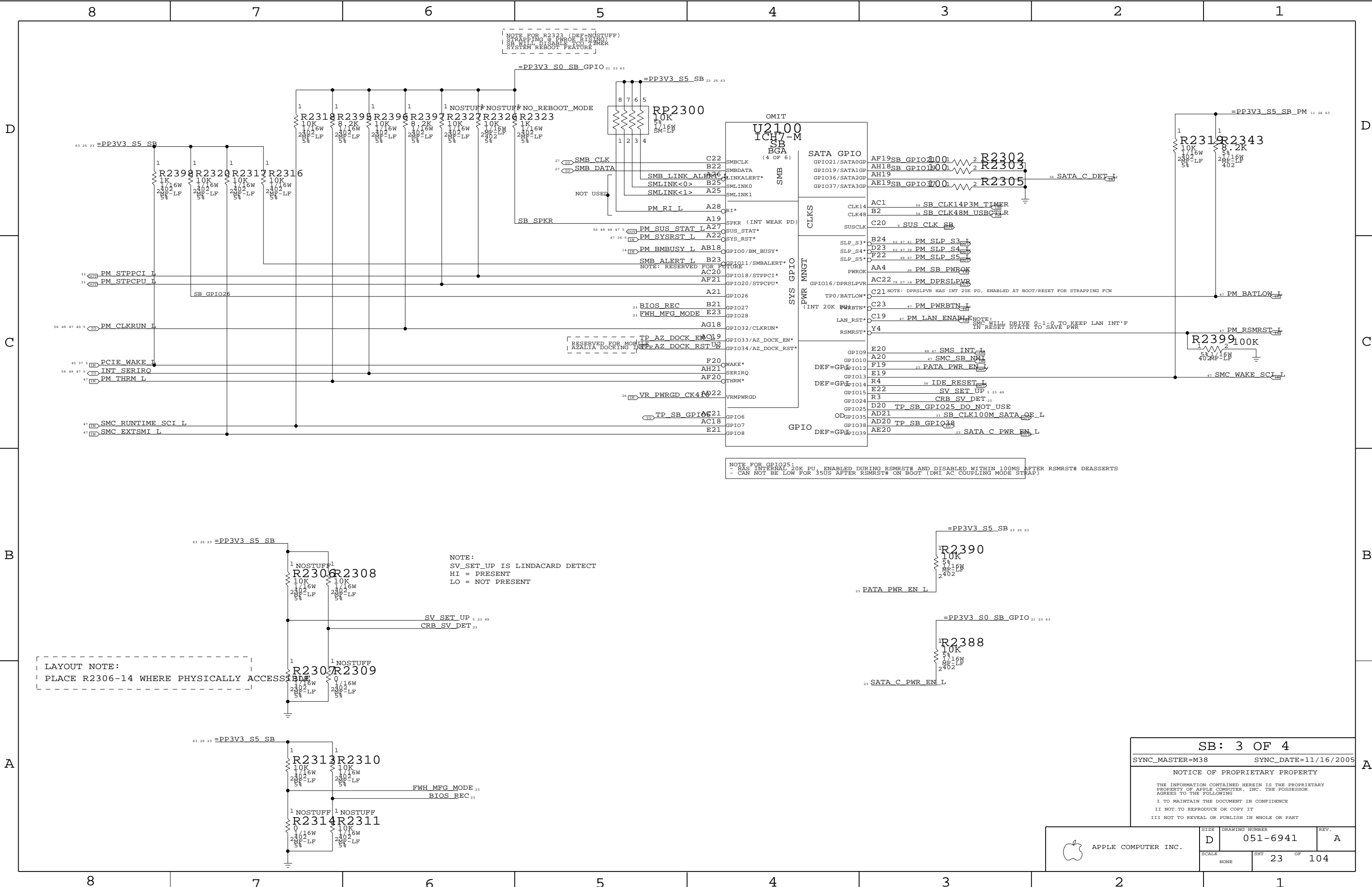
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. A
	SCALE NONE	SHT 17	OF 104







NOTE FOR R2323 (DEF=NOSTUFF):
STRAPPING @ FWRK RISING:
SB WILL DISABLE FCO TIMER
SYSTEM REBOOT FEATURE

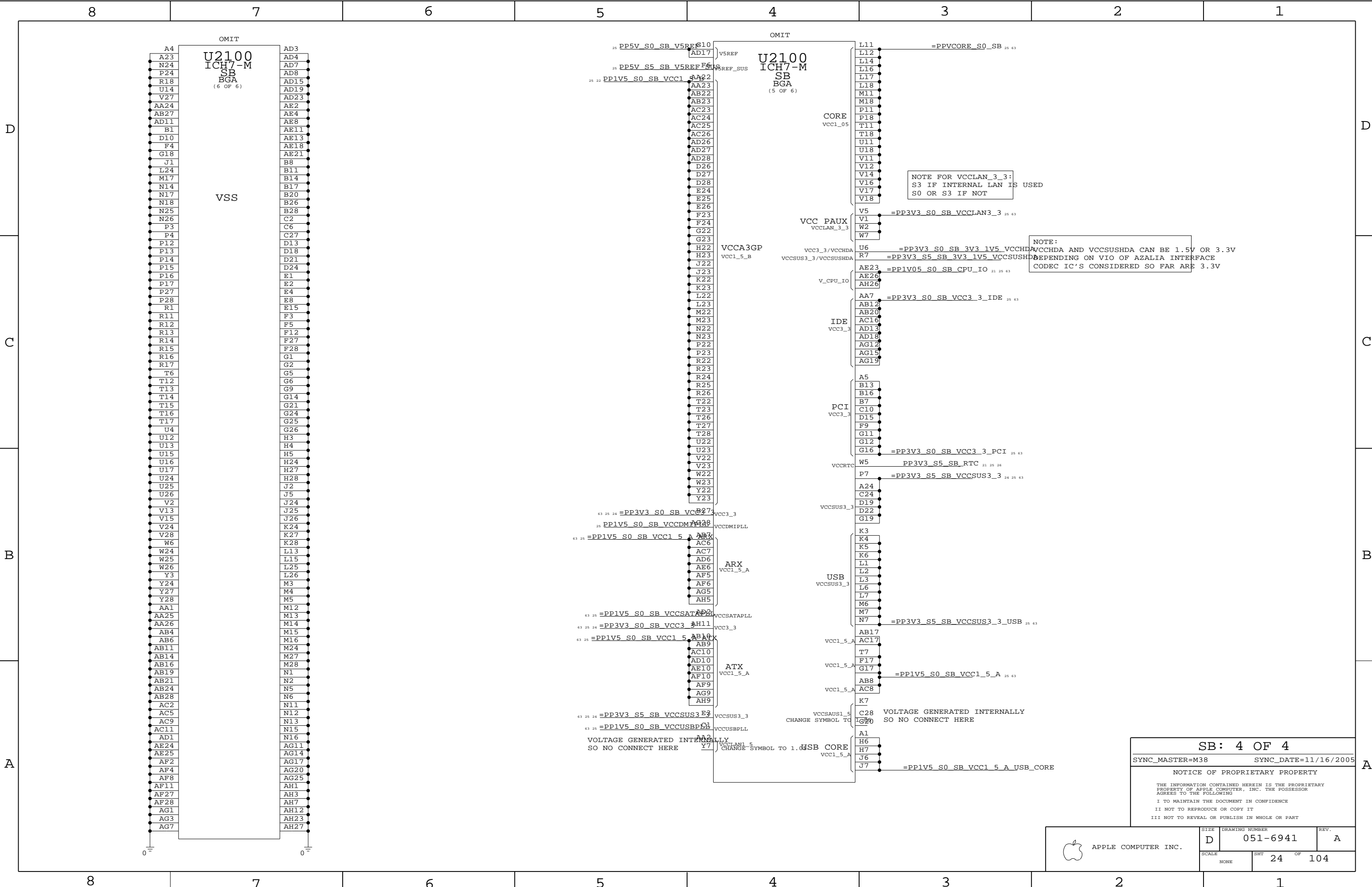
NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

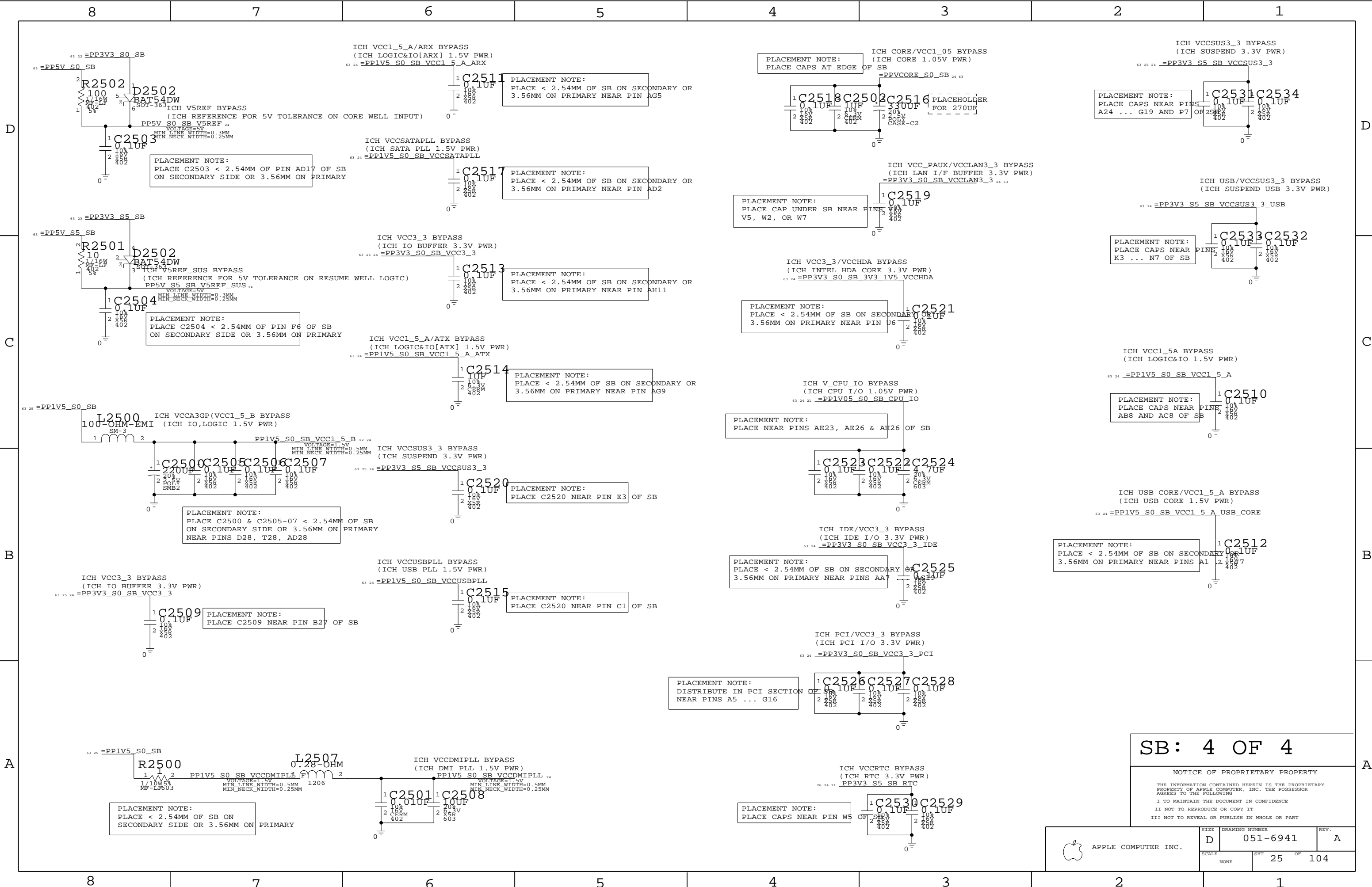
LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

SB: 3 OF 4
SYNC_MASTER=M38 SYNC_DATE=11/16/2005
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DRAWING NUMBER 051-6941
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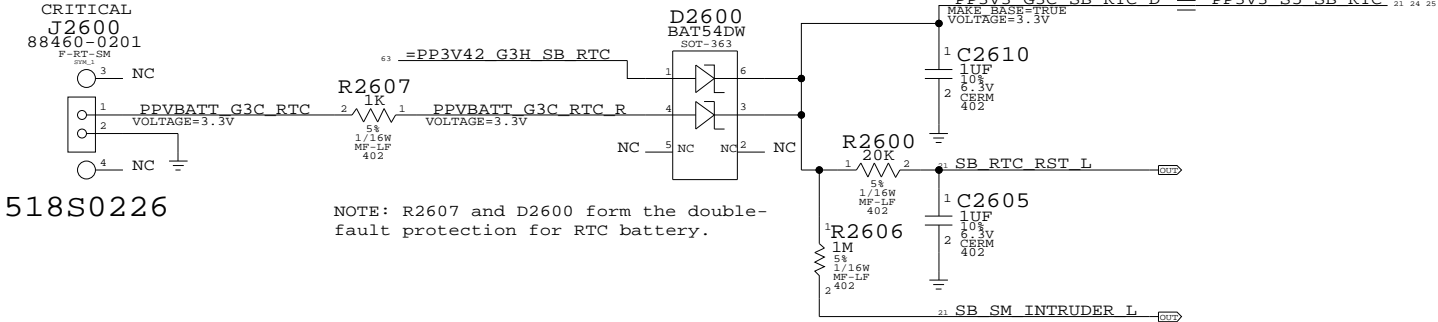
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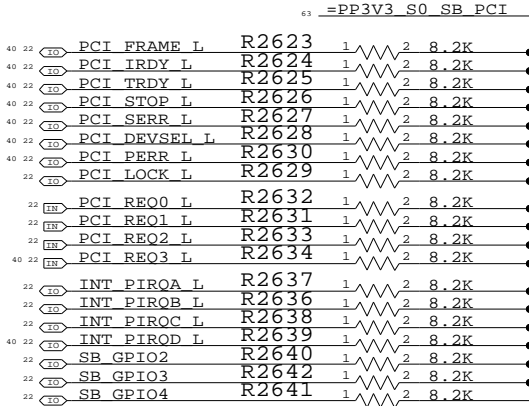
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE		SHT	25 OF 104
NONE			

RTC Battery Connector

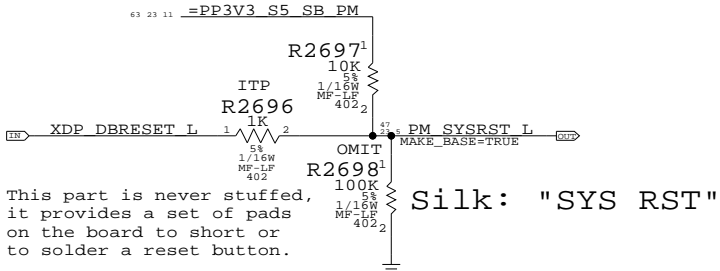
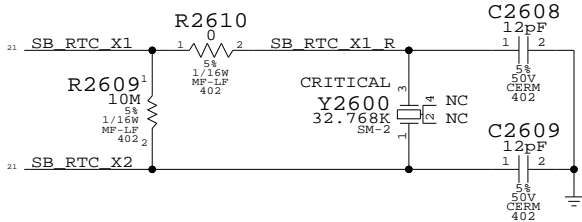


518S0226

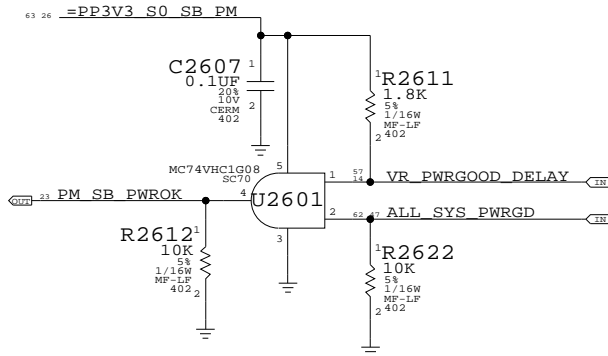
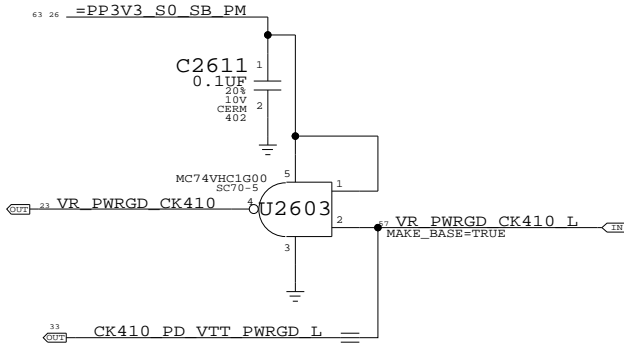
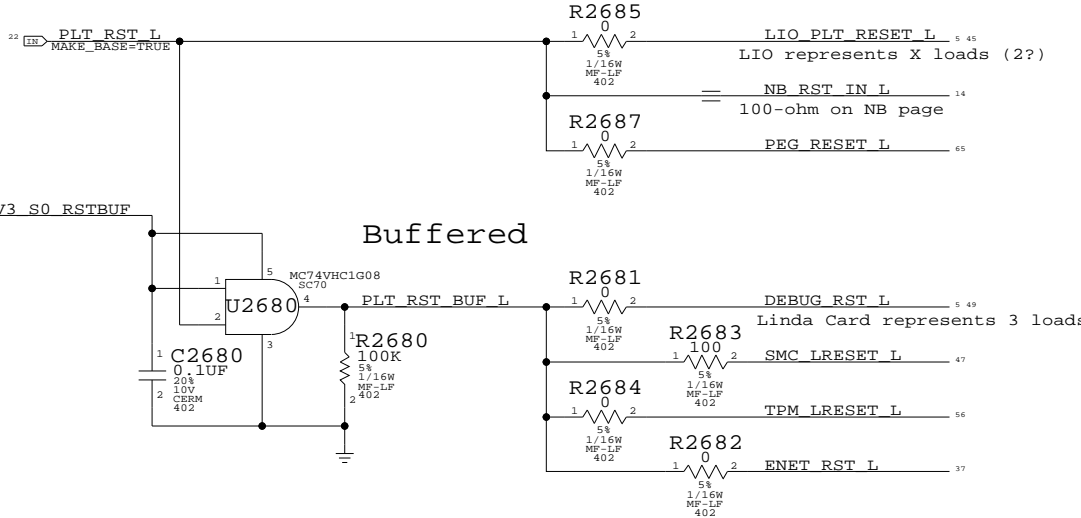
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



Platform Reset Connections
Unbuffered



1G00 used as small & cheap inverter

SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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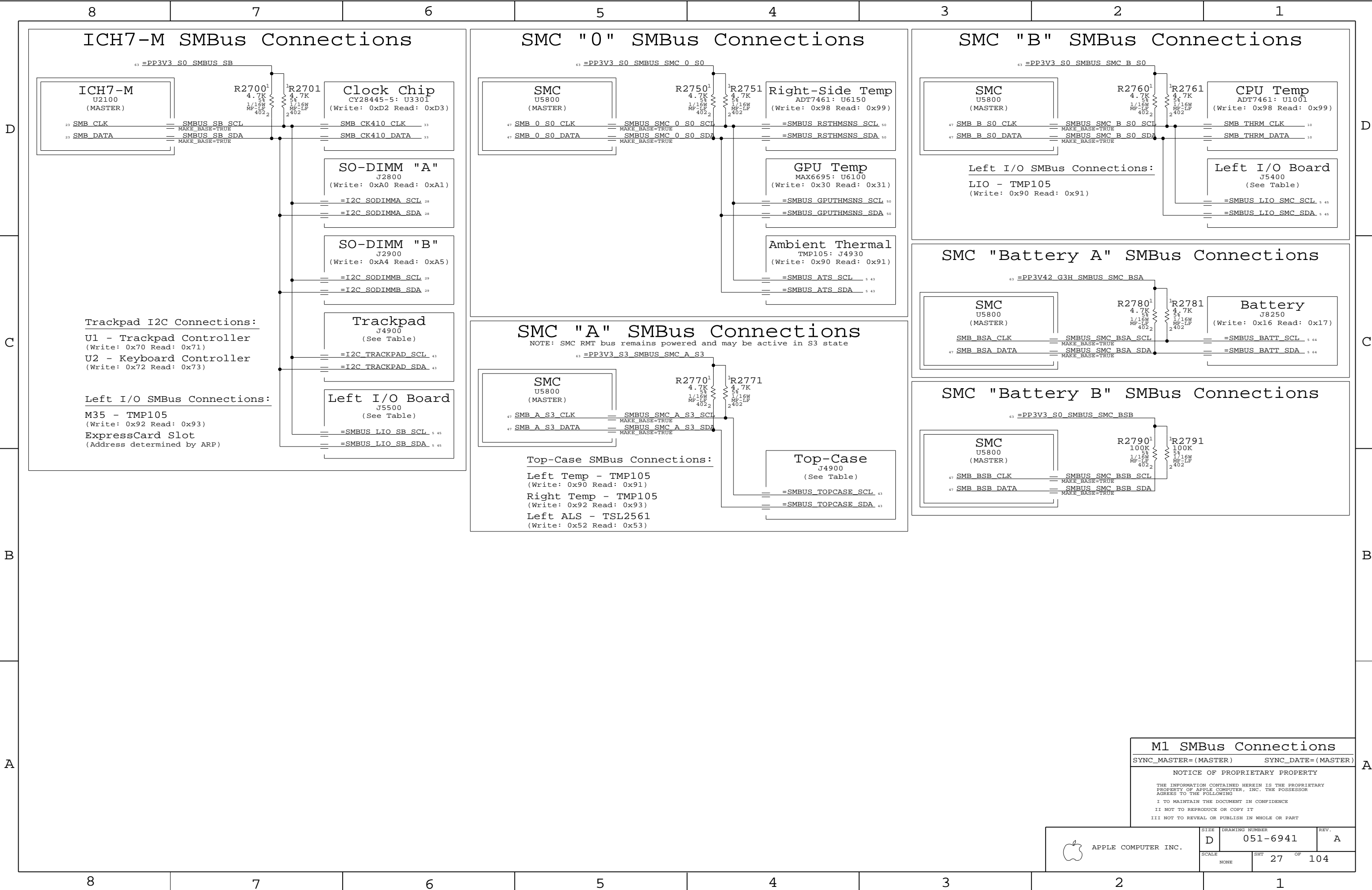
APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D 051-6941 A

SCALE SHT OF

NONE 26 104



M1 SMBus Connections

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

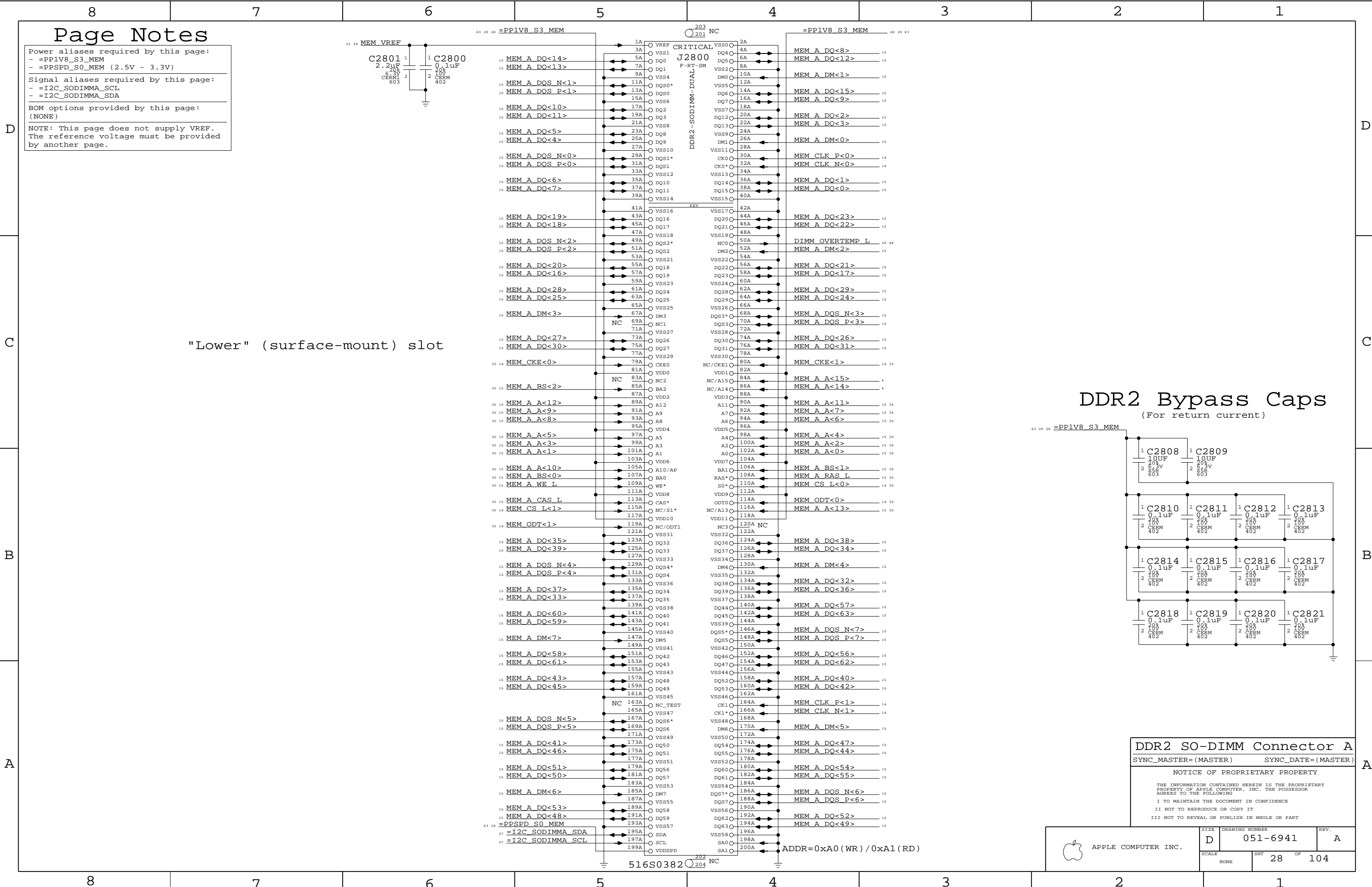
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"Lower" (surface-mount) slot

DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE

DRAWING NUMBER

REV.

SCALE

NONE

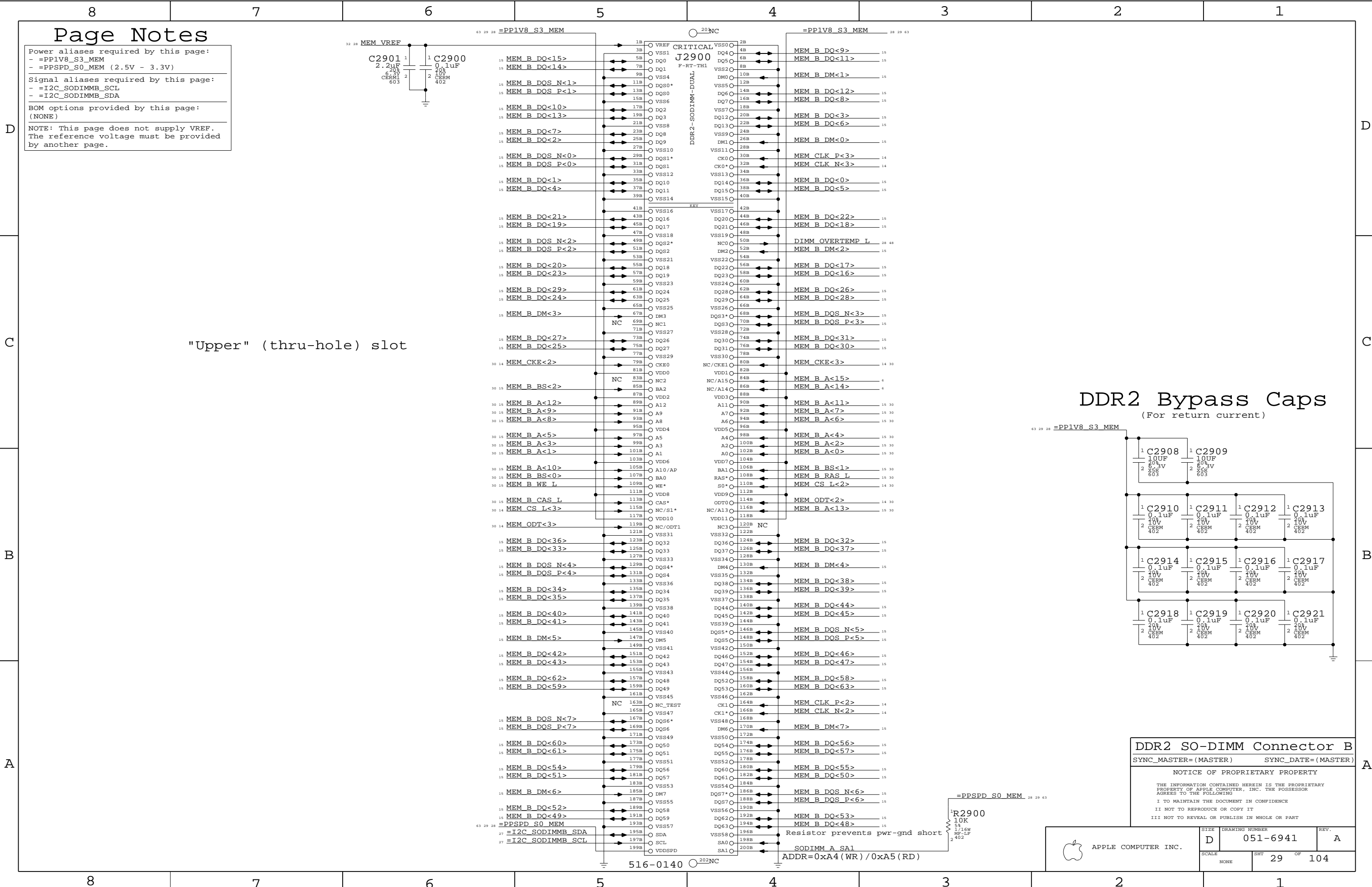
SHT

28

OF

104

A



Page Notes

Power aliases required by this page:
- =P1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

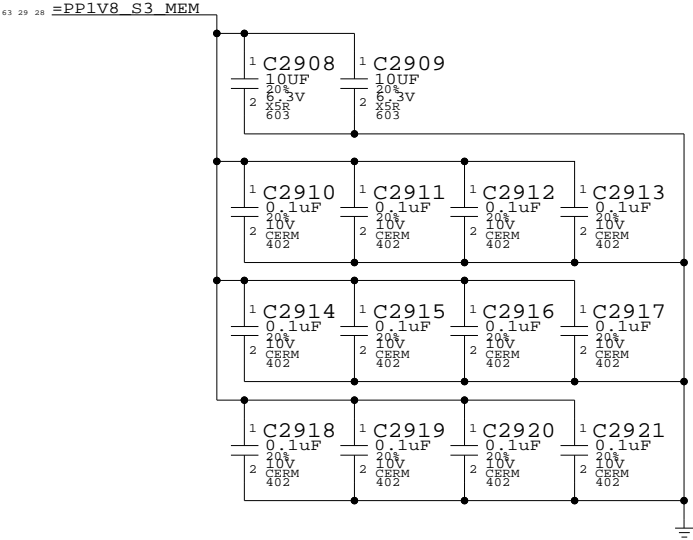
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Upper" (thru-hole) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

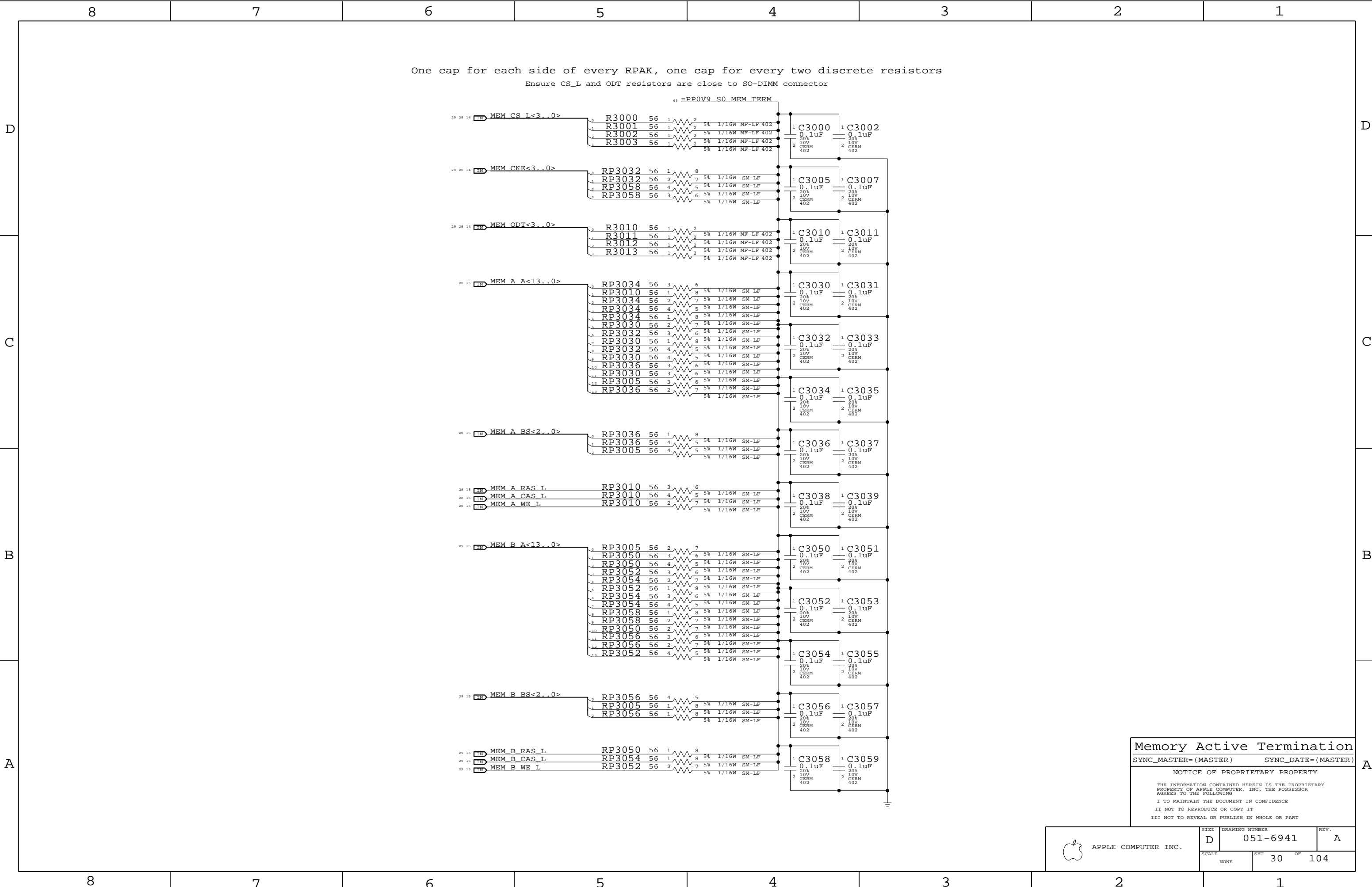
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	SCALE NONE	SHT 29	OF 104



Memory Active Termination

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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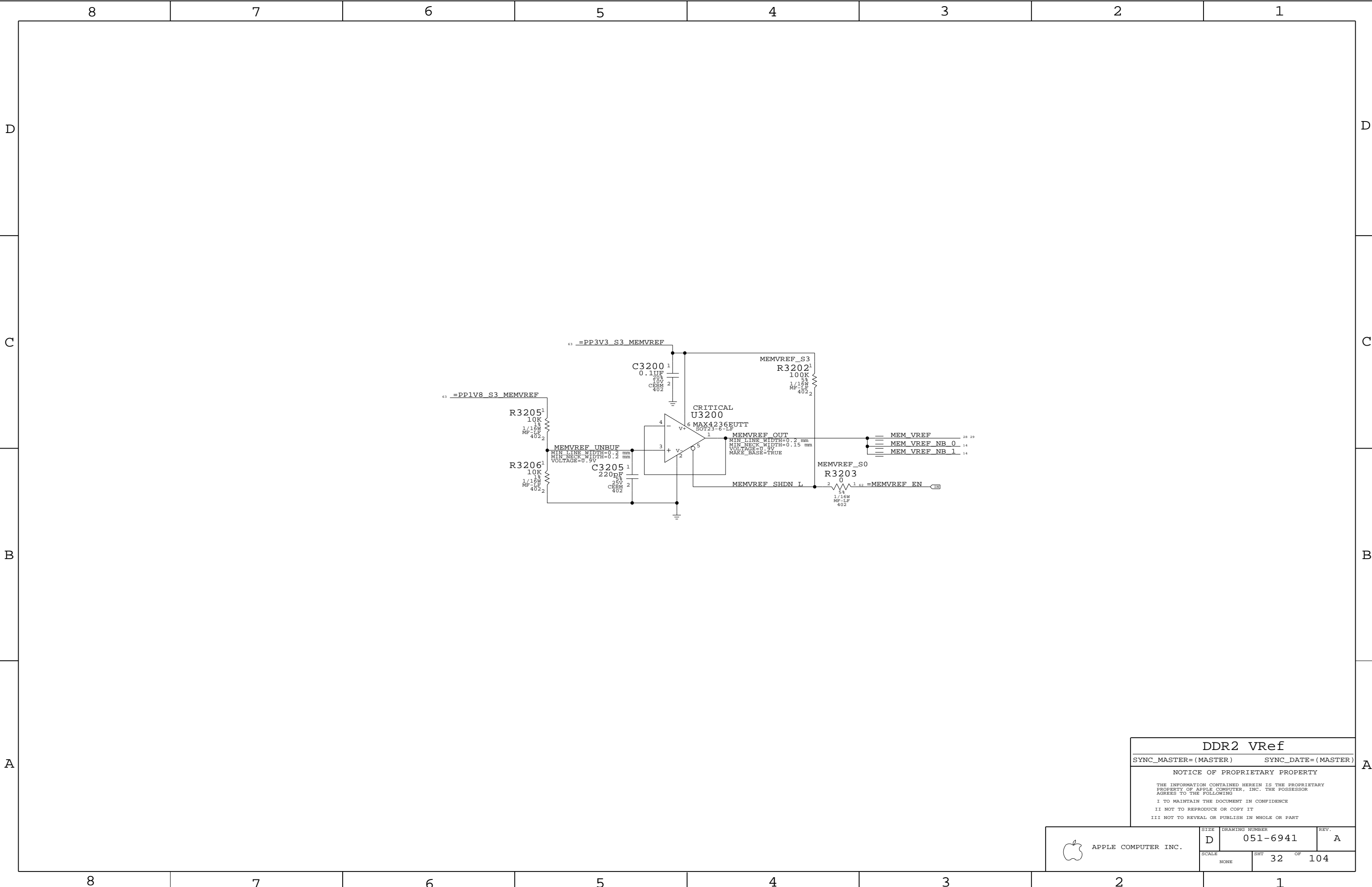
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-6941 REV. A

SCALE NONE SHT 30 OF 104



DDR2 Vref

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)


NOTICE OF PROPRIETARY PROPERTY

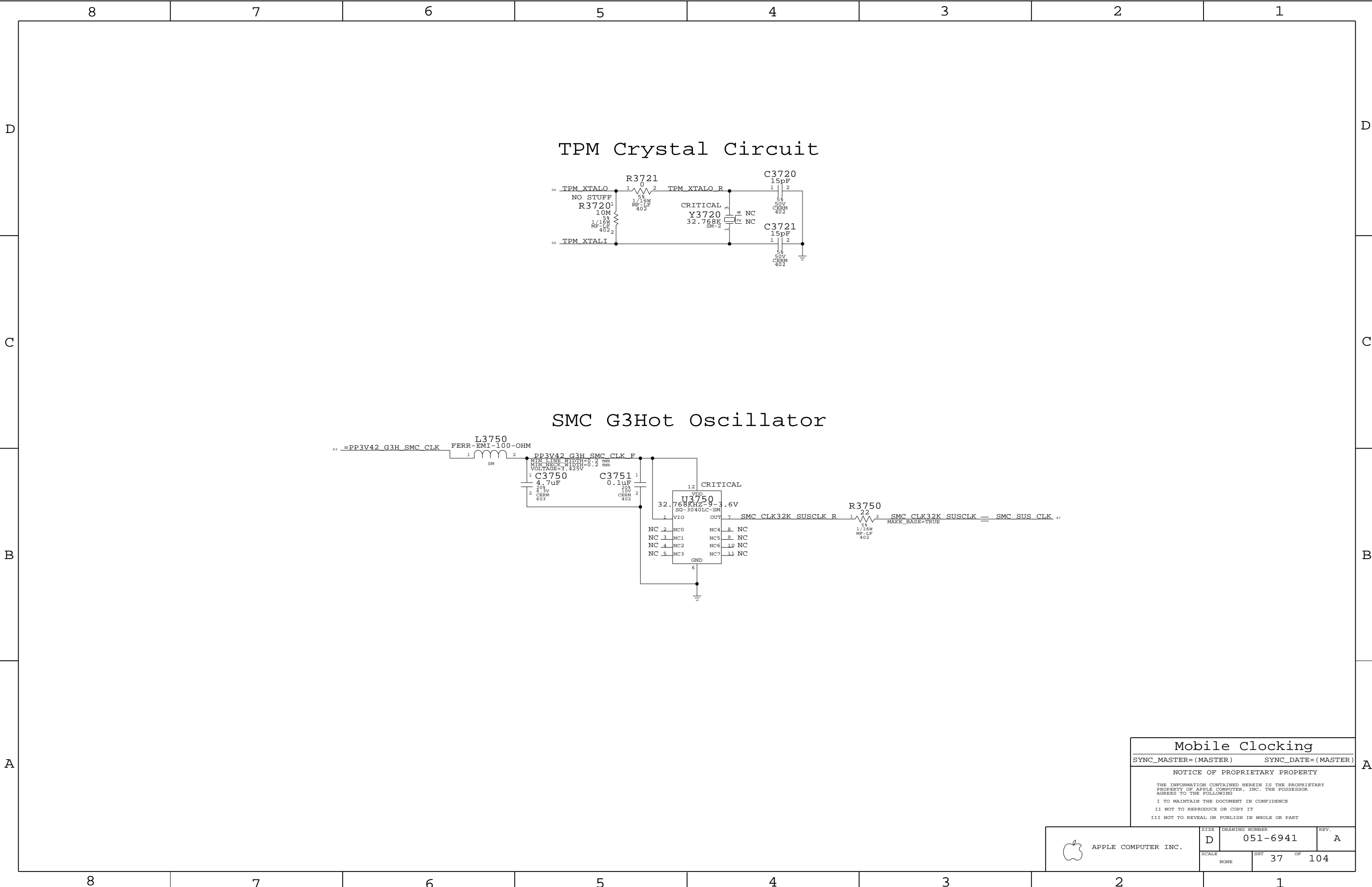
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	D	051-6941		A
SCALE		SHT	OF	
NONE		32	104	



Mobile Clocking

SYNC_MASTER= (MASTER)

SYNC_DATE= (MASTER)


NOTICE OF PROPRIETARY PROPERTY

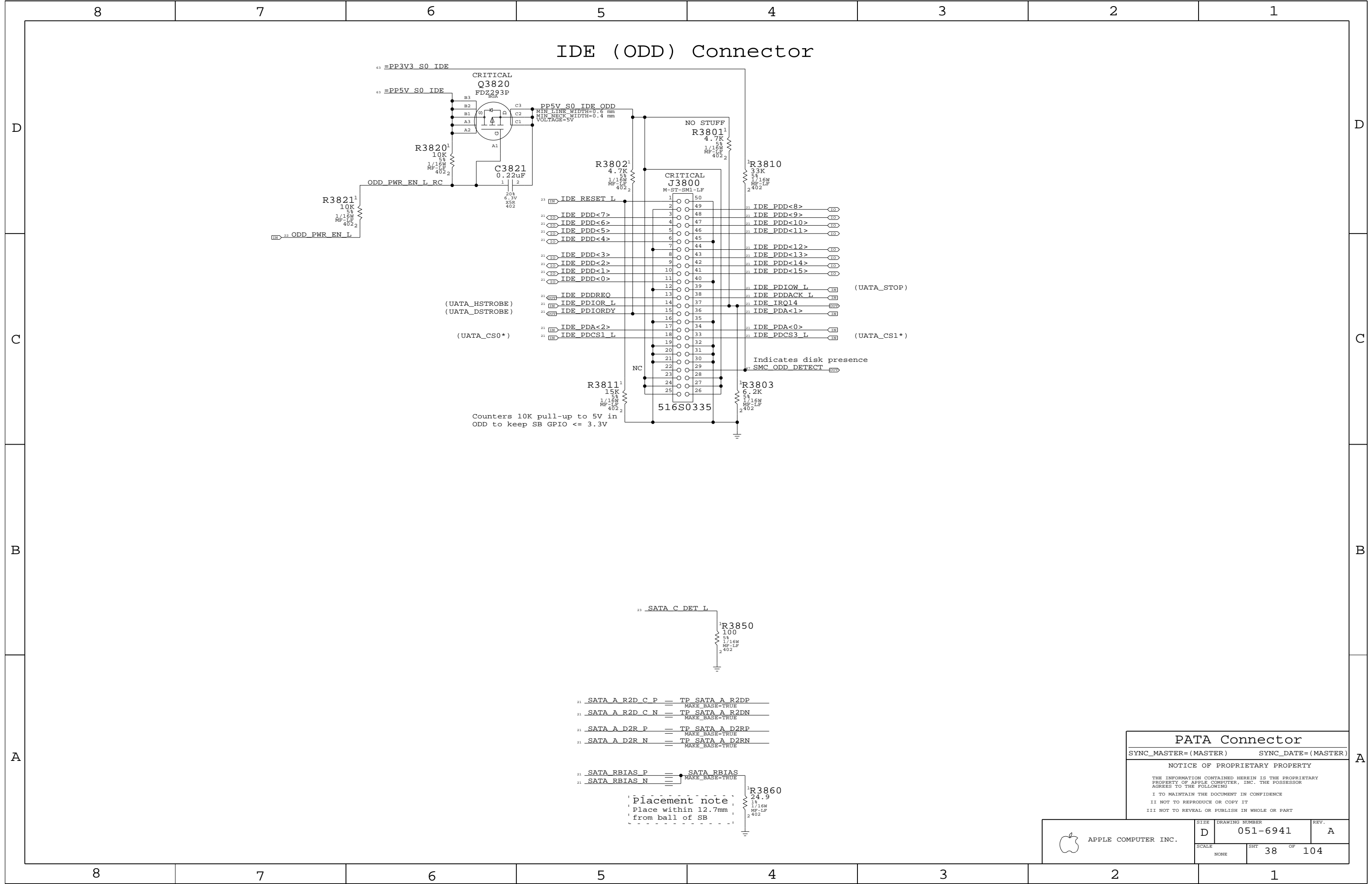
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	SCALE NONE	SHT 37	OF 104



PATA Connector

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

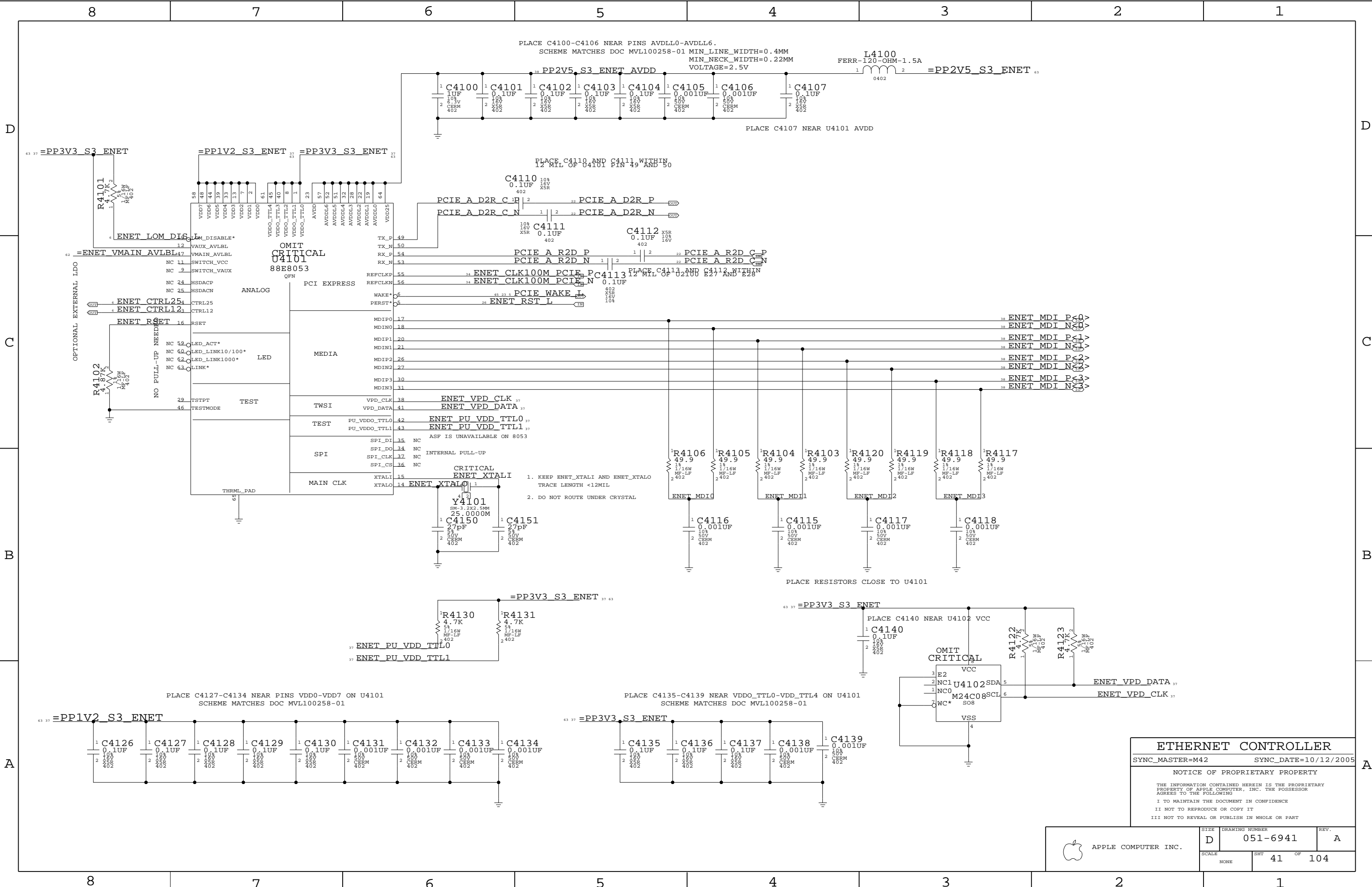
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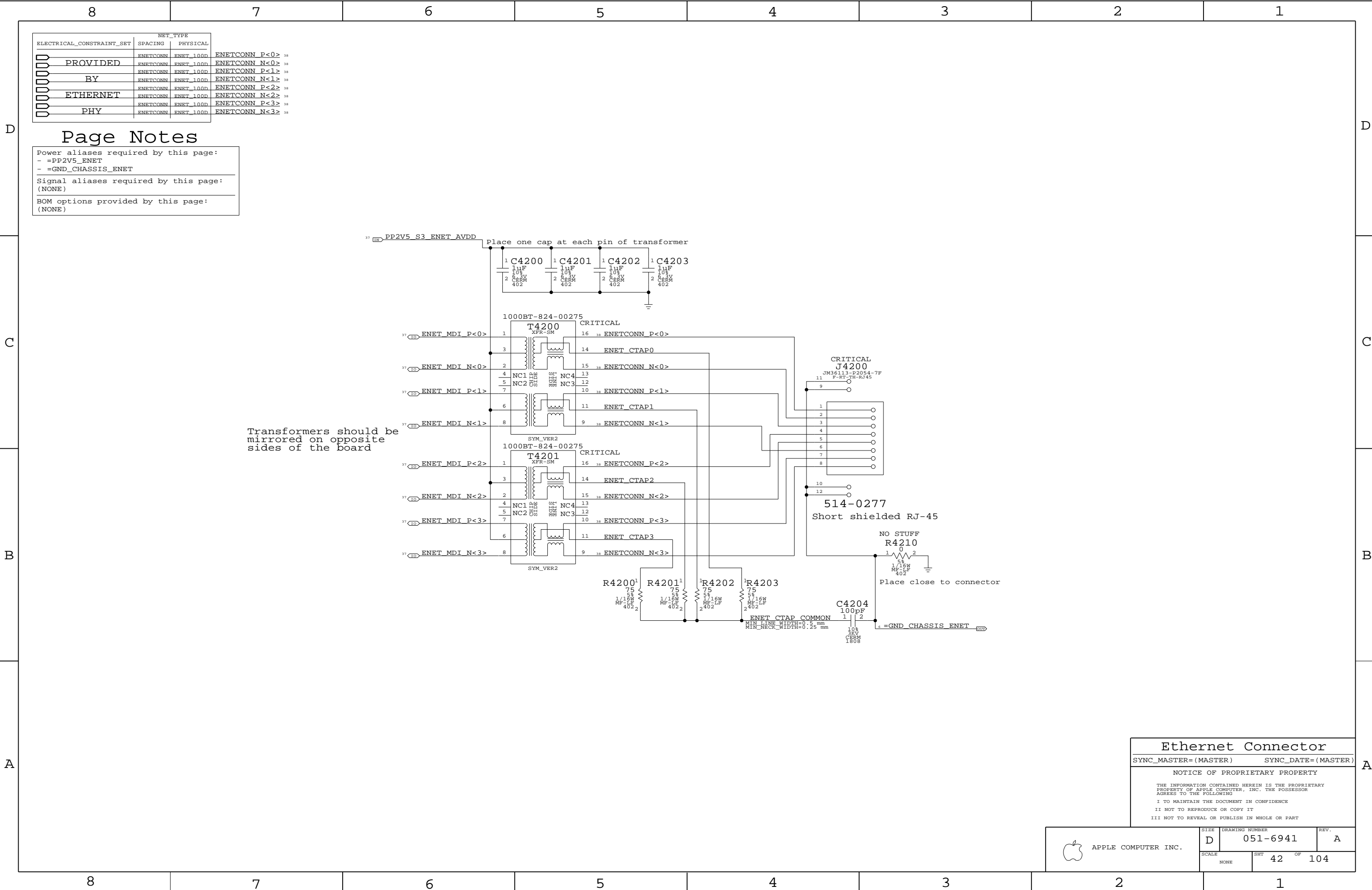
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. A
	SCALE NONE	SHT 38	OF 104



ETHERNET CONTROLLER		
SYNC_MASTER=M42		SYNC_DATE=10/12/2005
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NONE		41	104



Ethernet Connector

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

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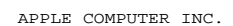
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	A
SCALE	NONE	SHT	42 OF 104

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DCB λ

```

INPUT
=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PCO - FIREWIRE POWER CLASS IDENTIFIER

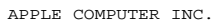
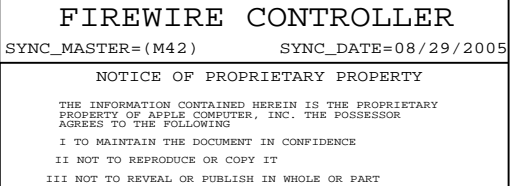
```

```
PCI_AD<0..31>, PCI_CBE_BE<0..3>, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L,
PCI_DEVSSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBAS - PORT 2 FIREWIRE DIFF PAIRS
```

```

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

```

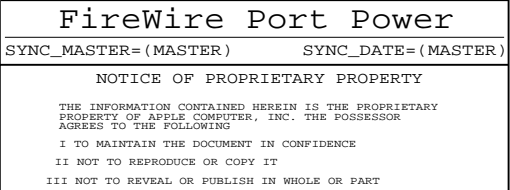
[illegible]

SIZE D	DRAWING NUMBER 051-6941	REV. A
SCALE NONE	SHT 44	OF 104

Power aliases required by this page:
 - =PPBUS_S0_FWPWSRW (system supply for bus power)
 - =PP3V3_S0_FWPORTPWSRW

Signal aliases required by this page:
 - =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
 (NONE)



ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	SPACING	PHYSICAL
PROVIDED	FW	FW_110D
BY	FW	FW_110D
PHY	FW	FW_110D
PAGE	FW	FW_110D

Page Notes

Power aliases required by this page:

- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:

(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

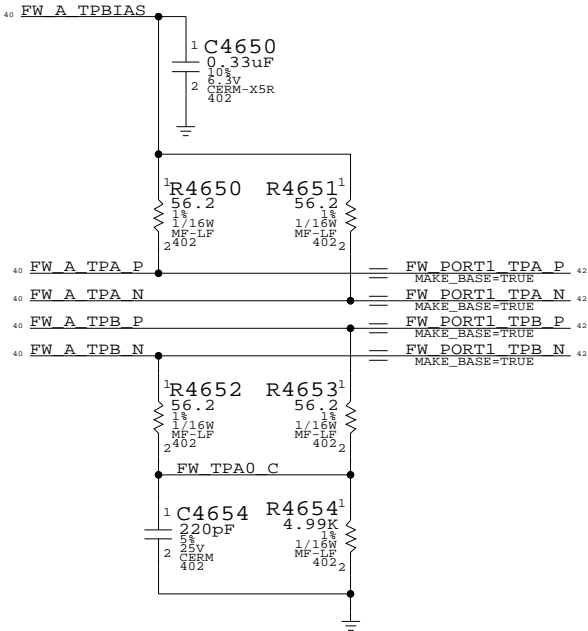
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

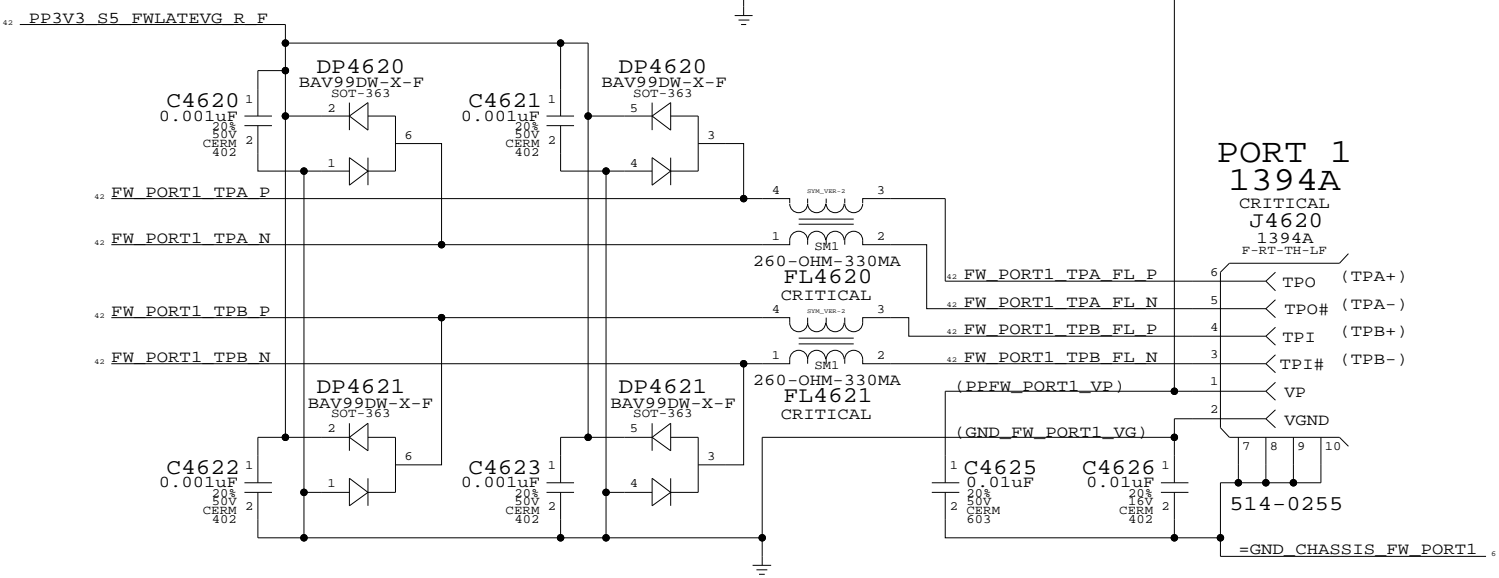
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

Place close to FireWire PHY



"Snapback" & "Late VG" Protection

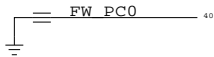


2nd TPA/TPB pair unused 3rd TPA/TPB pair unused

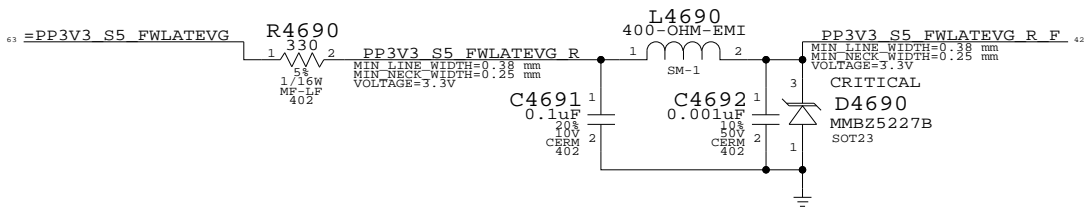


FW Power Class Strap

Single-port system sets PC=0

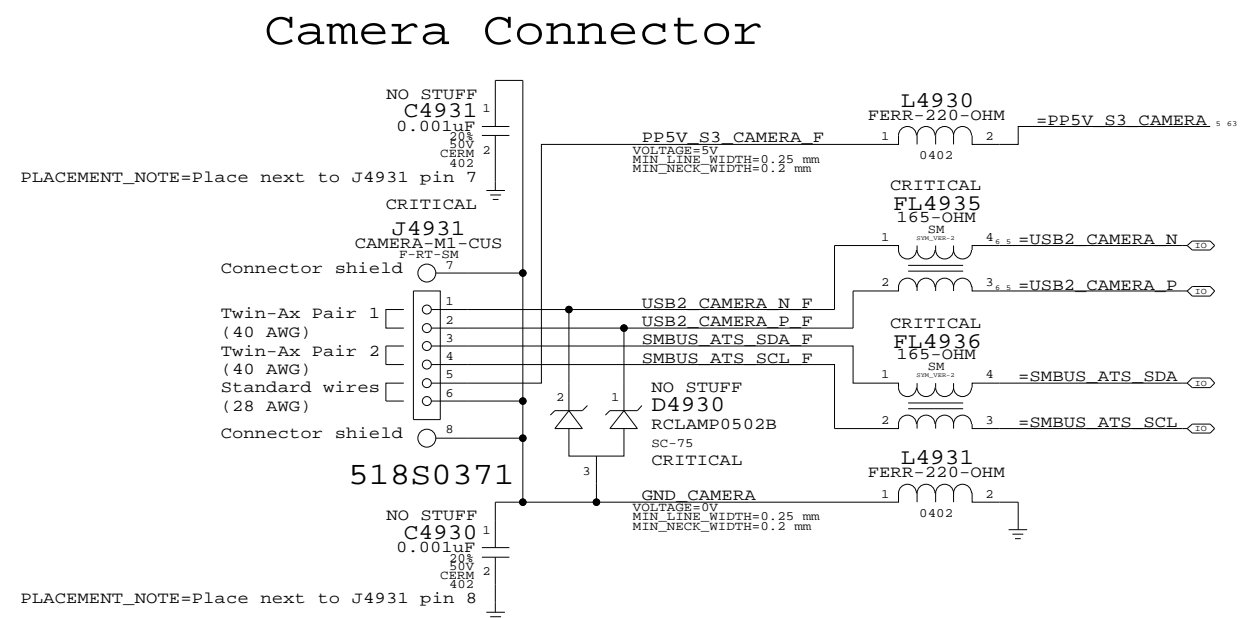
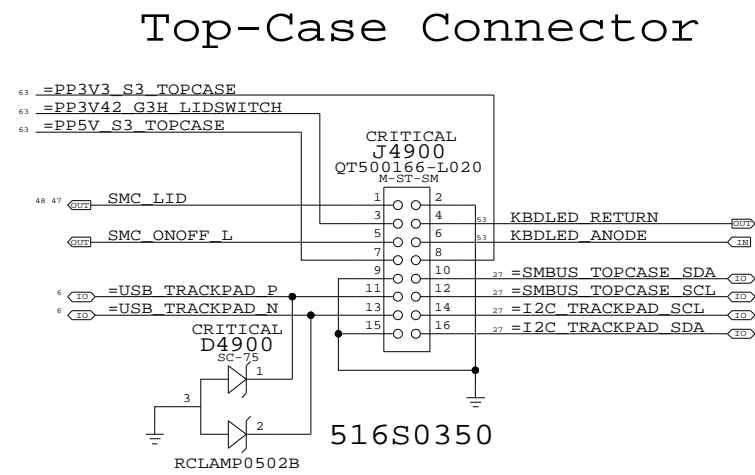


Late-VG Protection Power




FireWire Ports	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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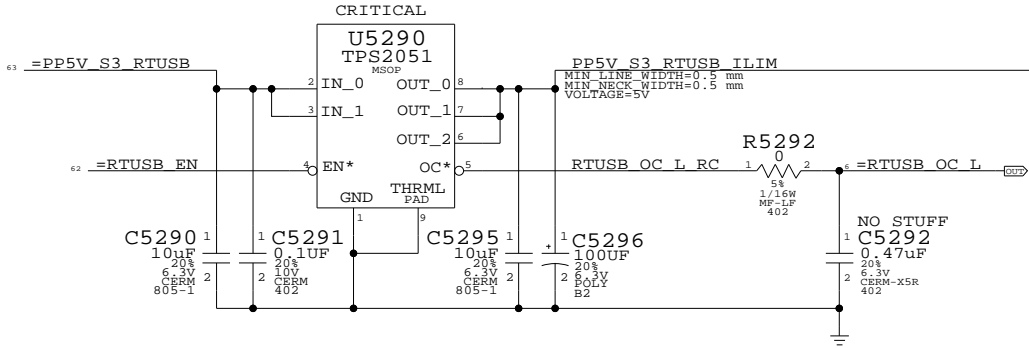
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	A
SCALE		SHT	OF
NONE		46	104



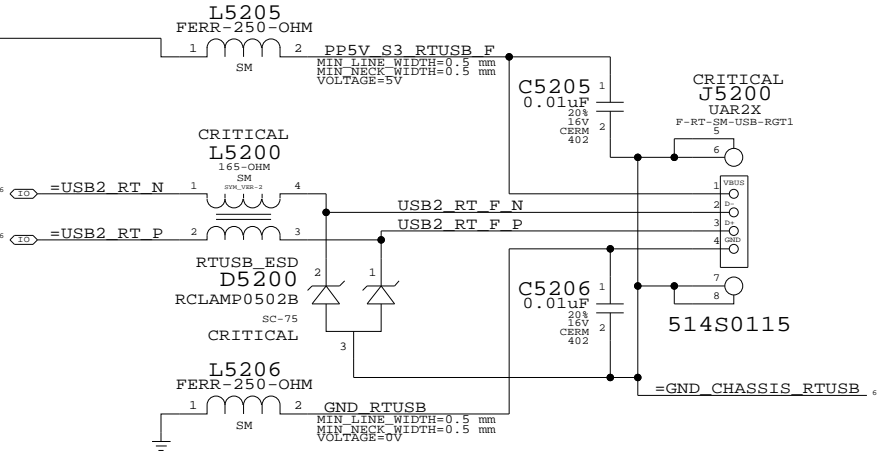
<h1>Internal USB Connections</h1>	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
<h2>NOTICE OF PROPRIETARY PROPERTY</h2>	
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	D	051-6941	A
	SCALE	SHT	OF
	NONE	49	104

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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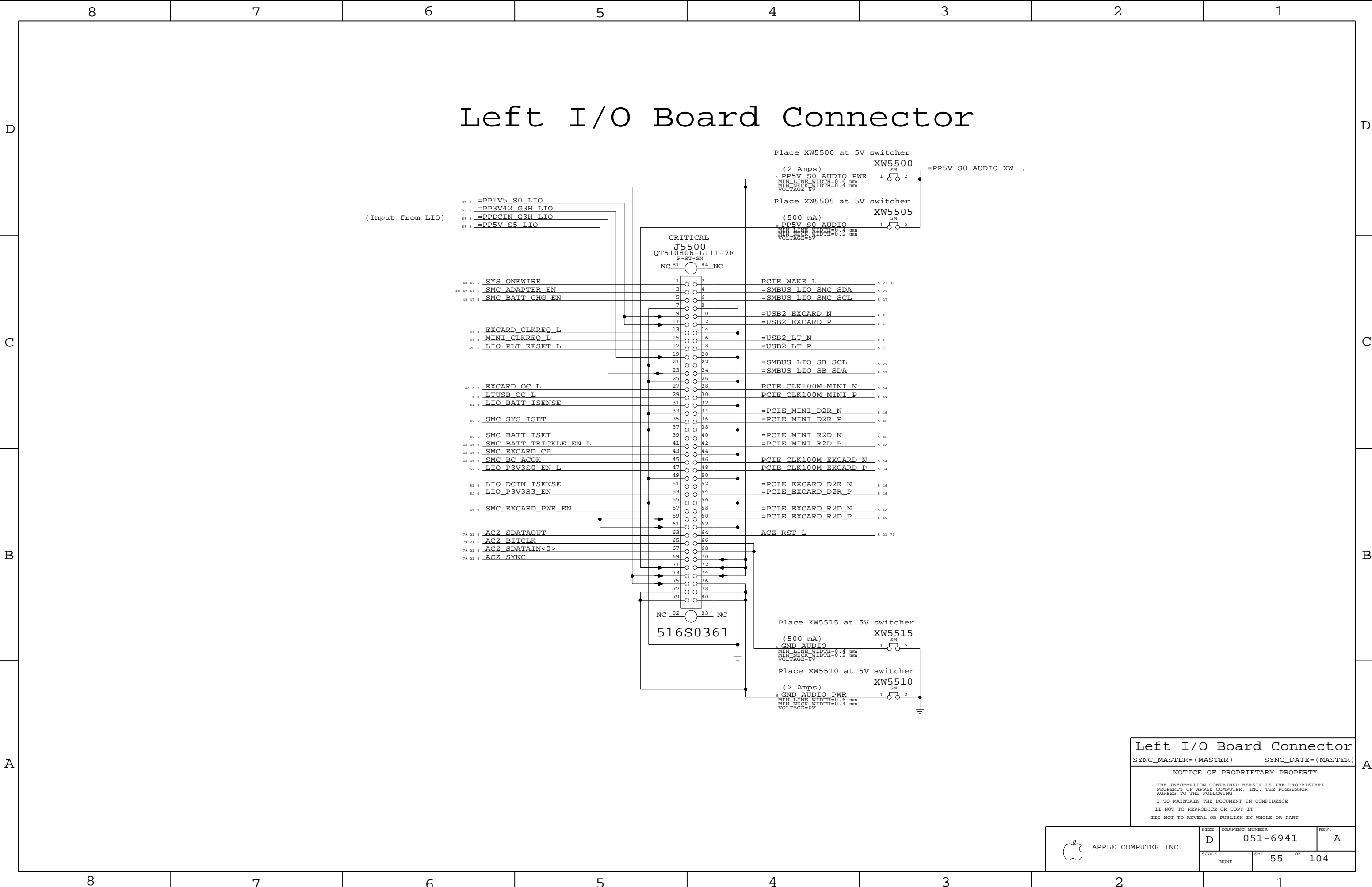
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SIZE D DRAWING NUMBER 051-6941 REV. A

SCALE NONE SHT 52 OF 104



Left I/O Board Connector

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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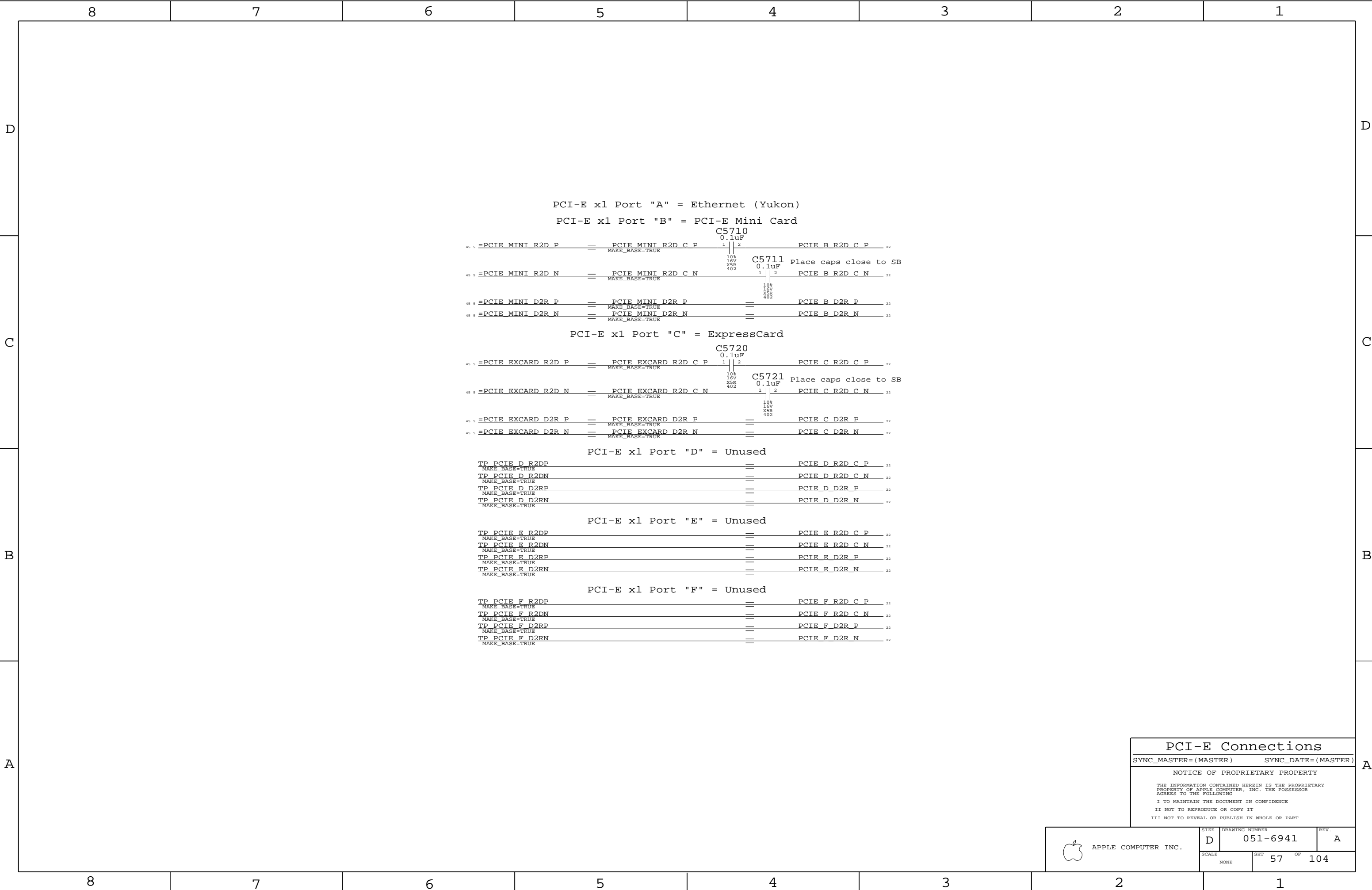
II NOT TO REPRODUCE OR COPY IT

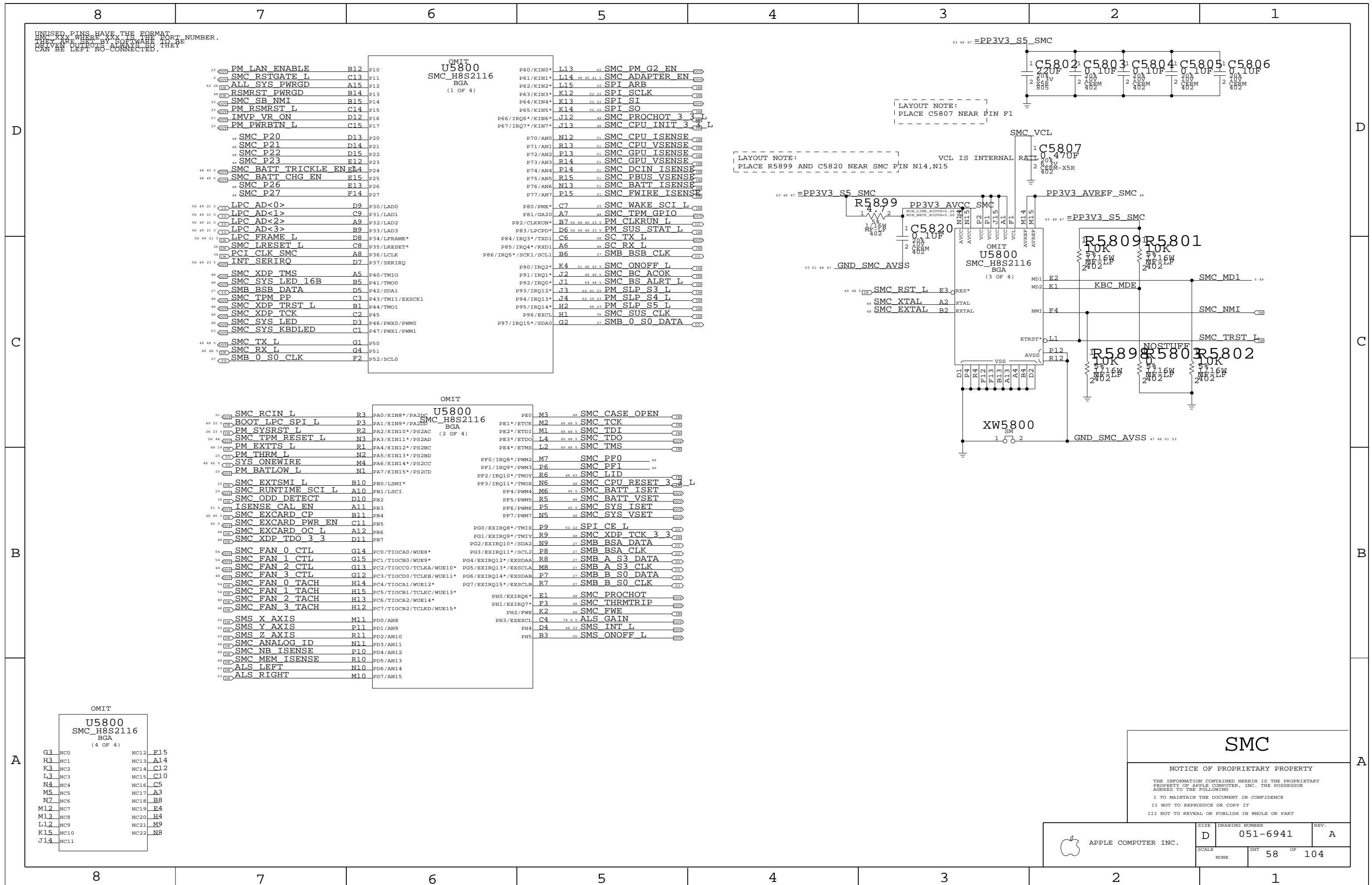
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

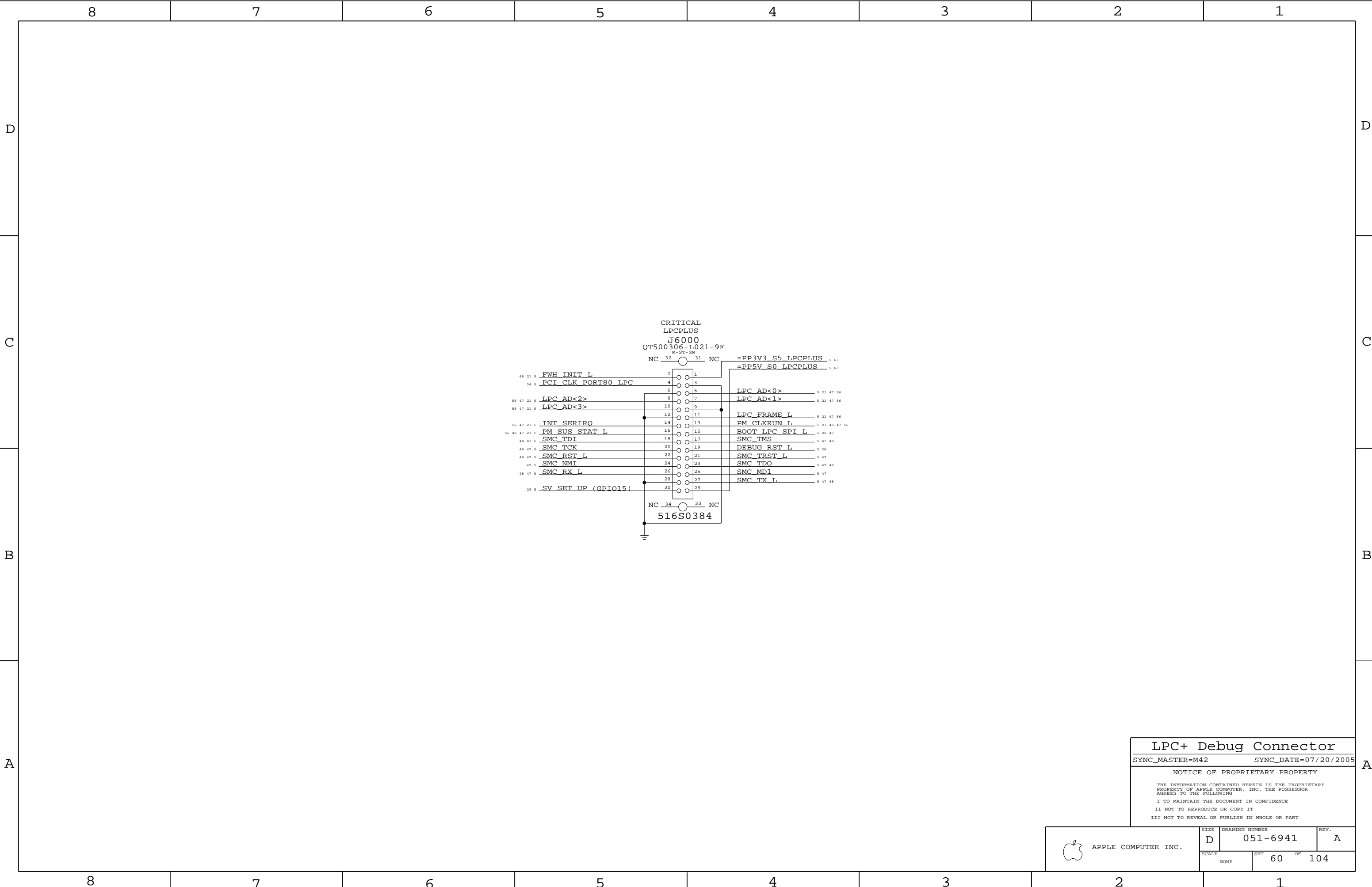


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SIZE	DRAWING NUMBER	REV.
D	051-6941	A
SCALE	SHT	OF
NONE	55	104







LPC+ Debug Connector

SYNC_MASTER=M42

SYNC_DATE=07/20/2005


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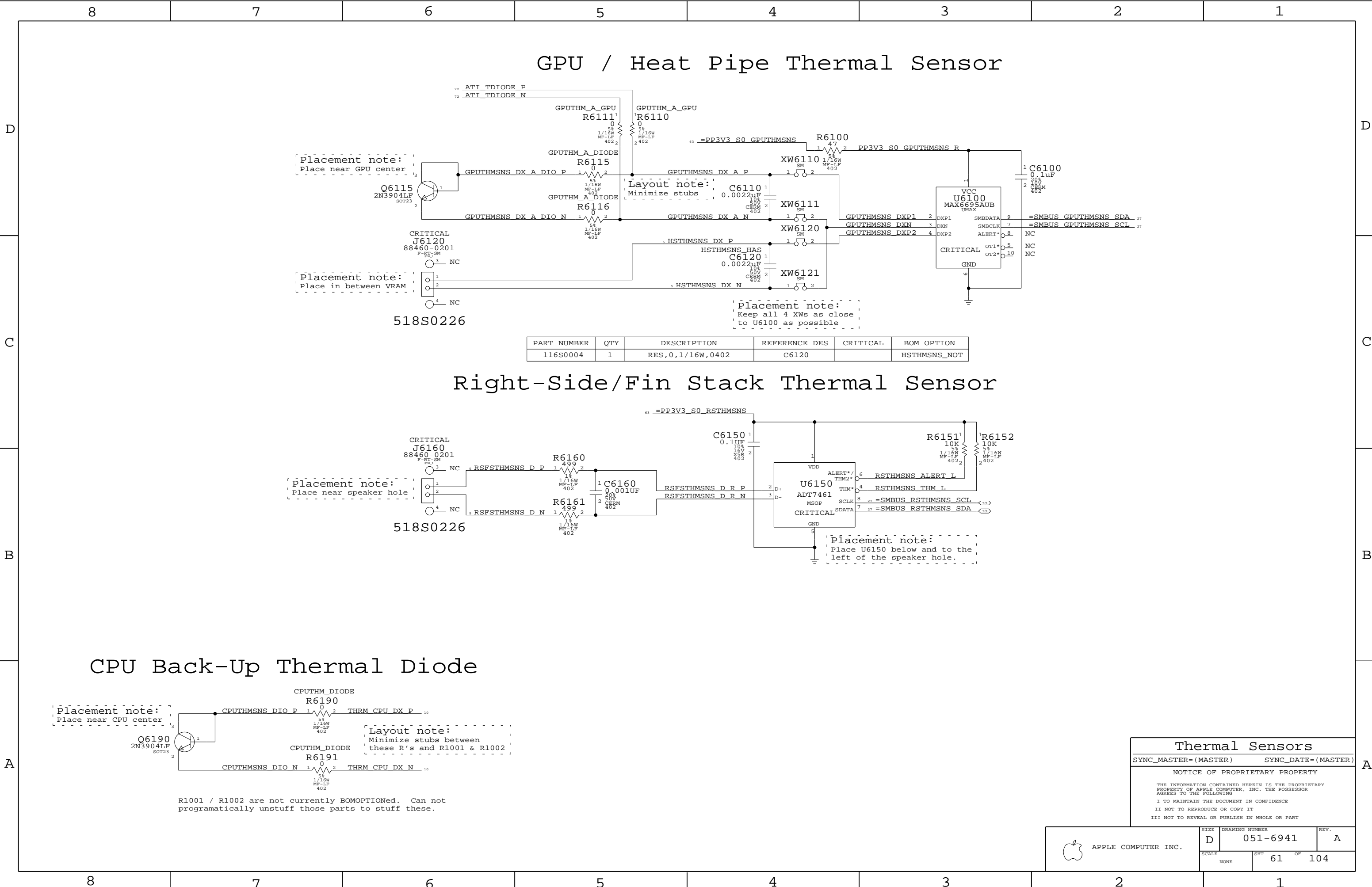
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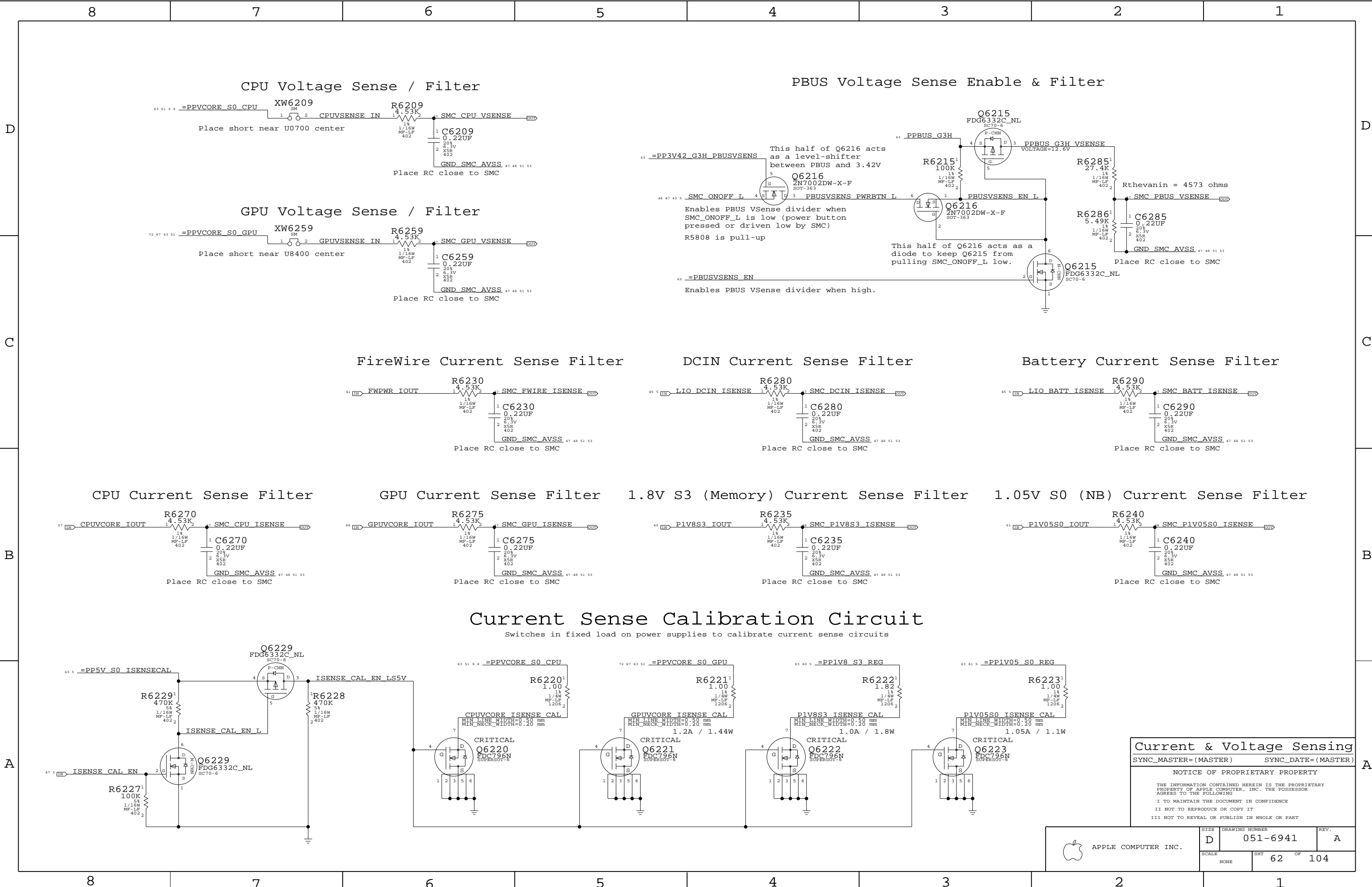
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

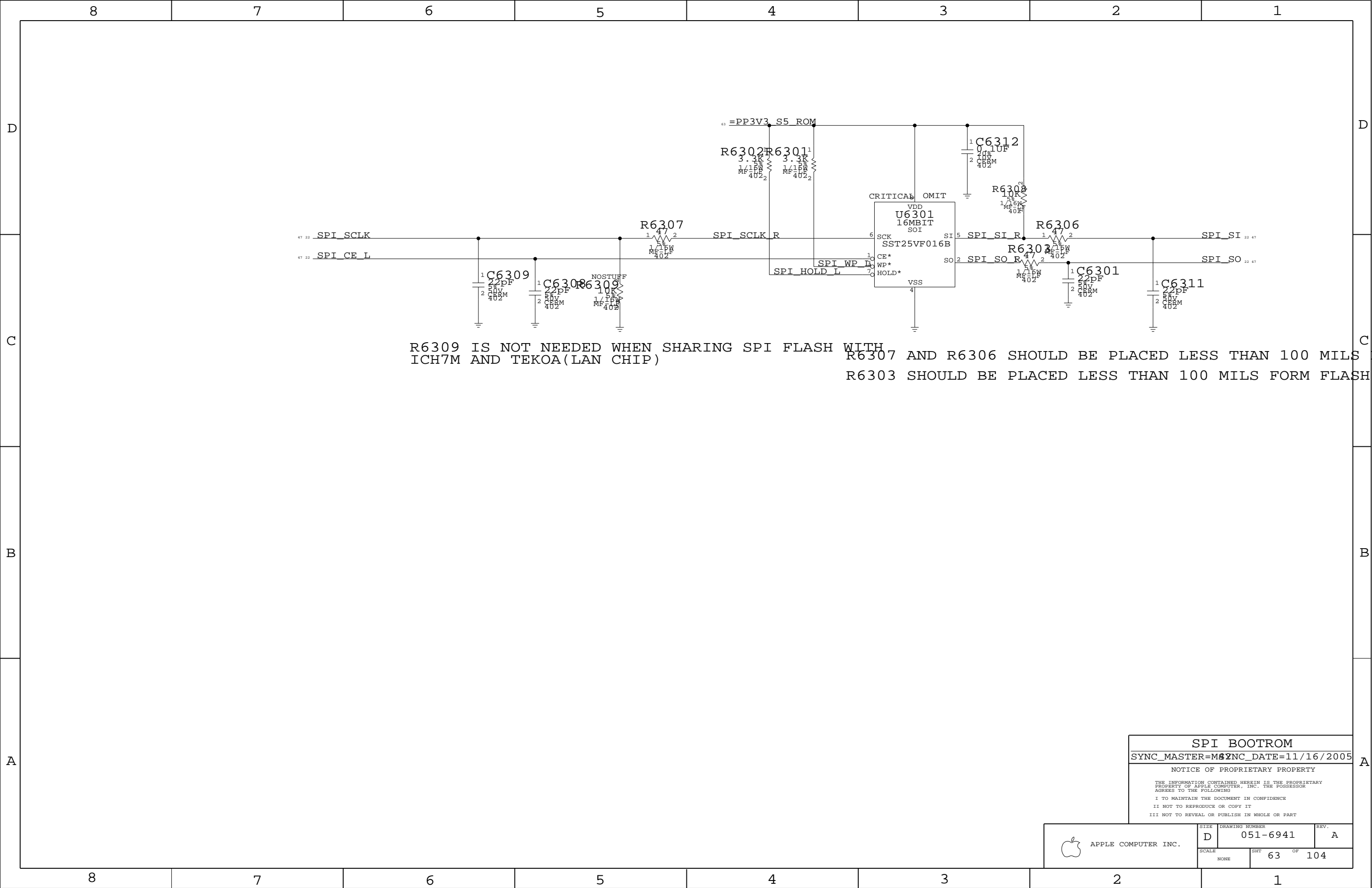
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	D	051-6941		A
SCALE		SHT	OF	
NONE		60	104	







R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=MSYNC_DATE=11/16/2005


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SCALE		SHT	OF
NONE		63	104

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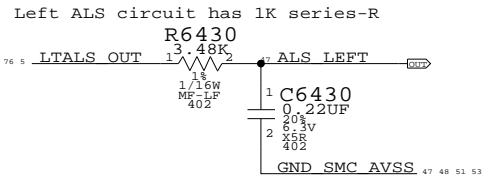
4

3

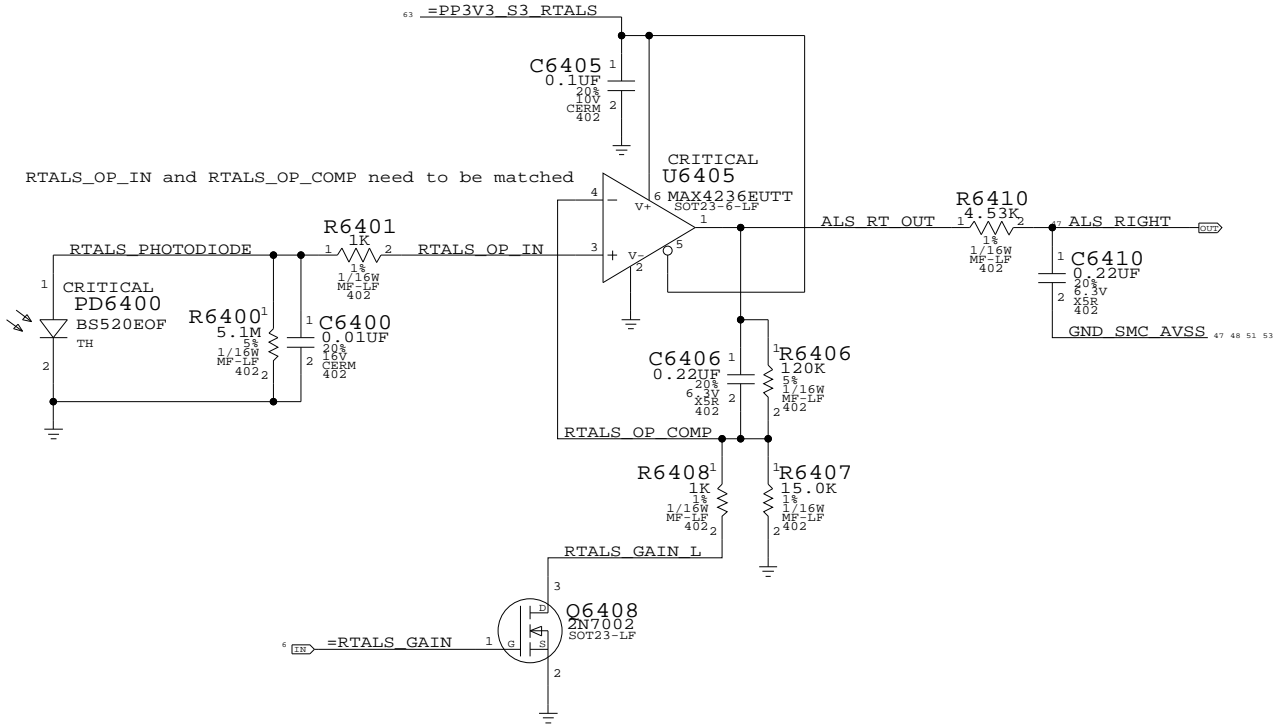
2

1

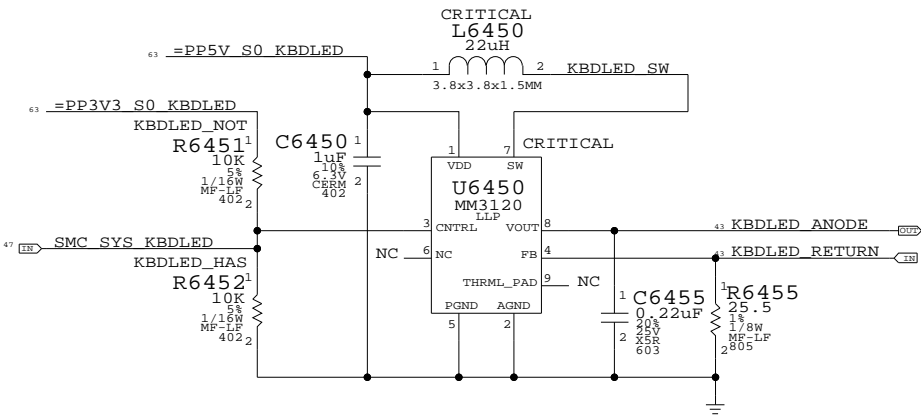
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

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NONE 64 104

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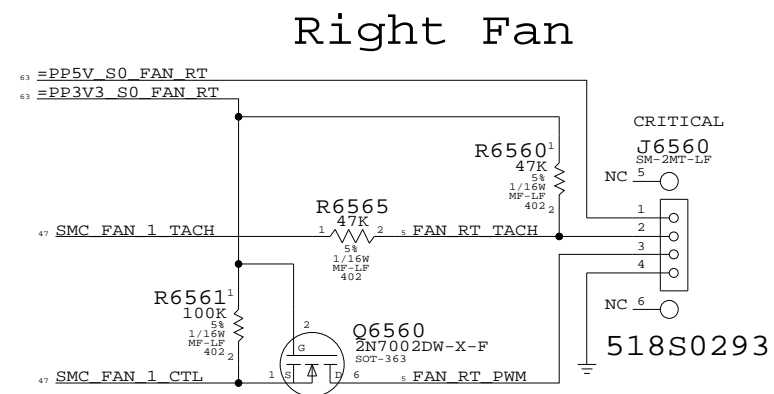
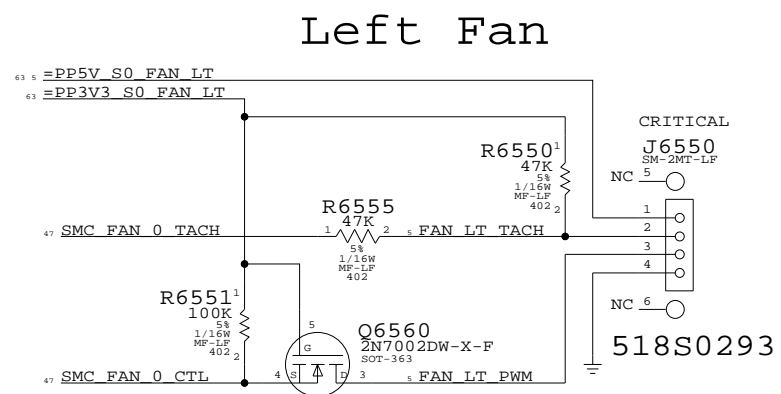
5

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Fan Connectors

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
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	SIZE
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SIZE	DRAWING NUMBER
D	051-6941

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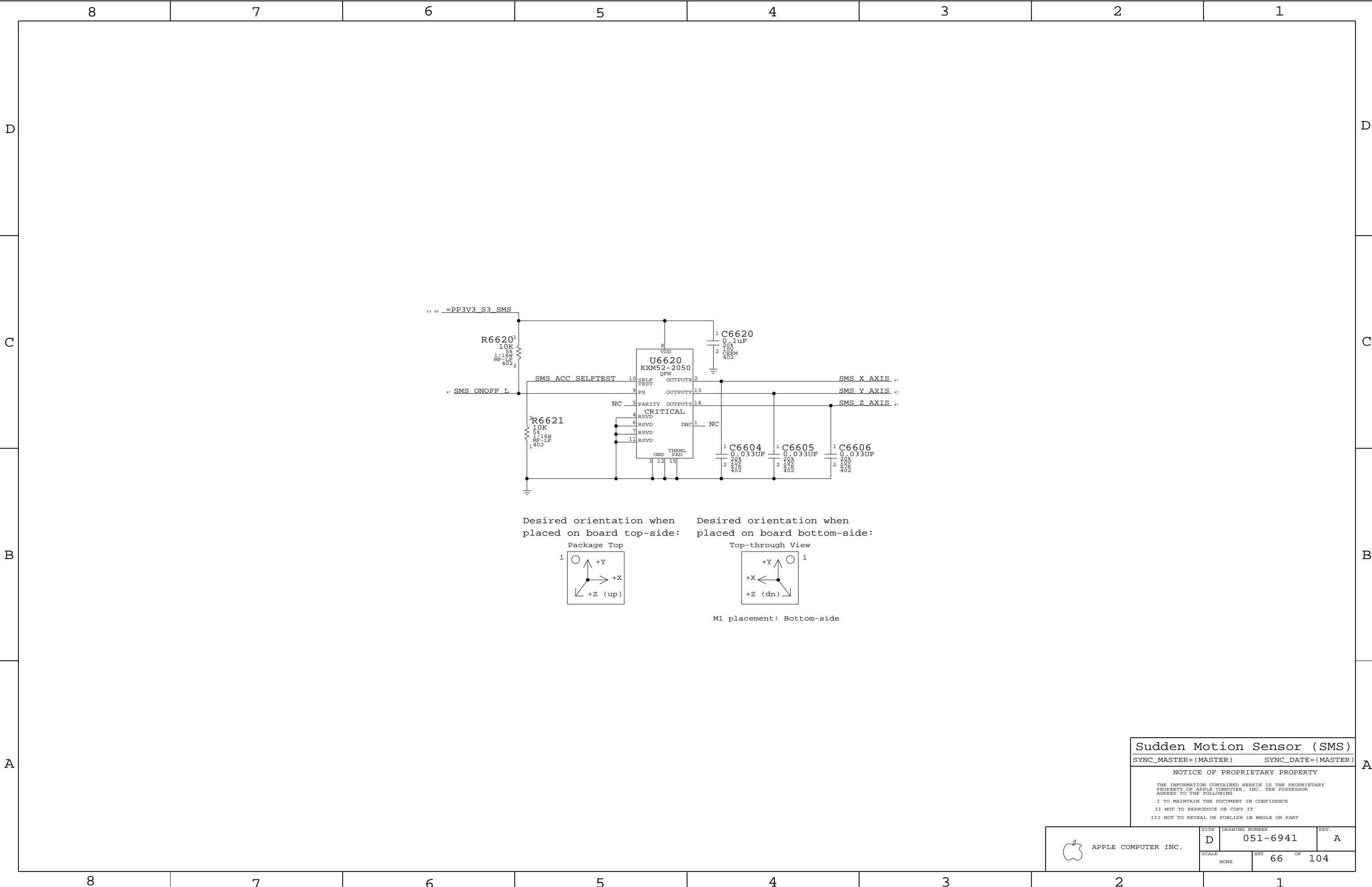
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65 OF 104

65 104



Sudden Motion Sensor (SMS)

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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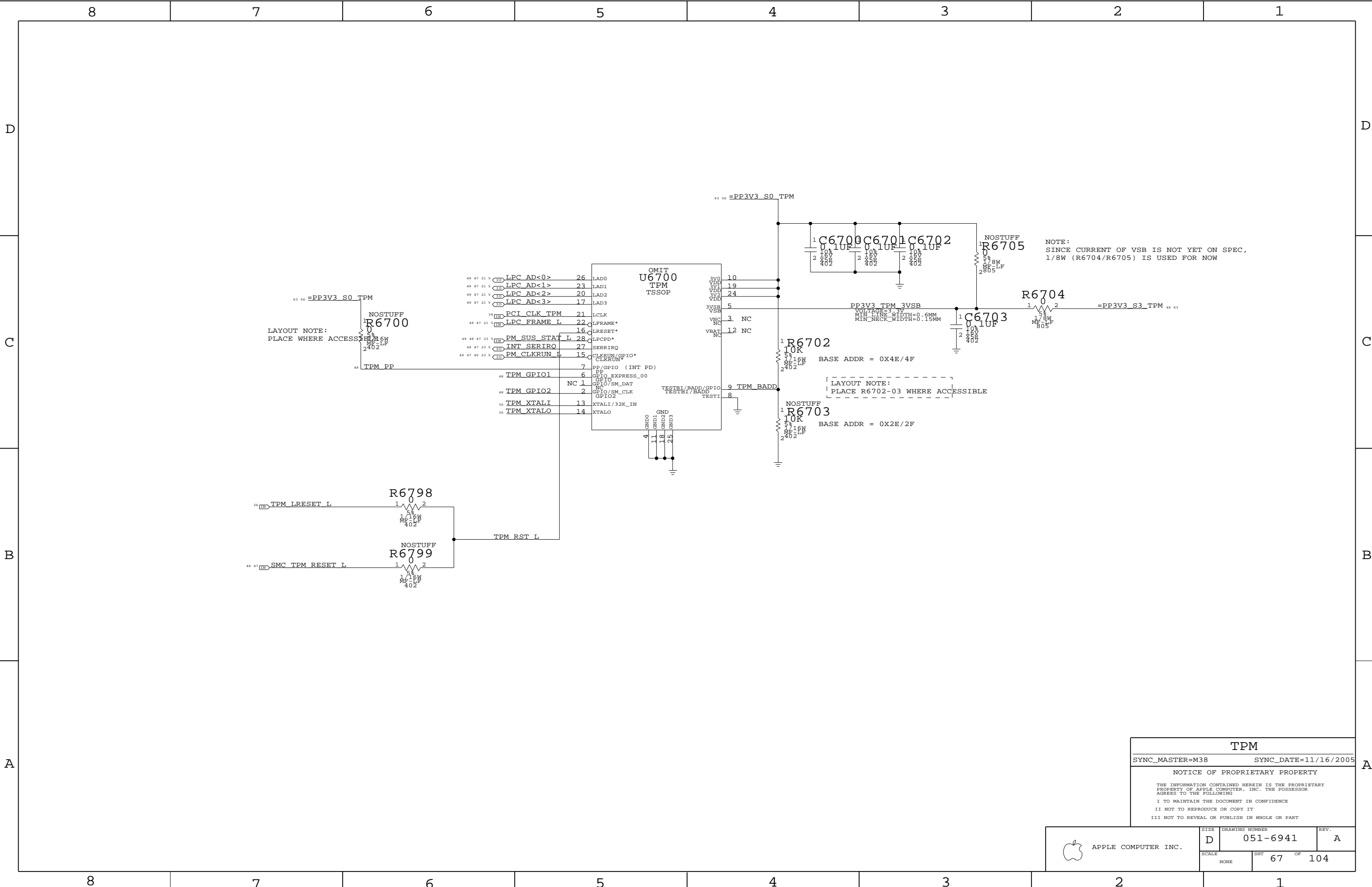
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	SCALE NONE	SHT 66	OF 104



TPM

SYNC_MASTER=M38

SYNC_DATE=11/16/2005

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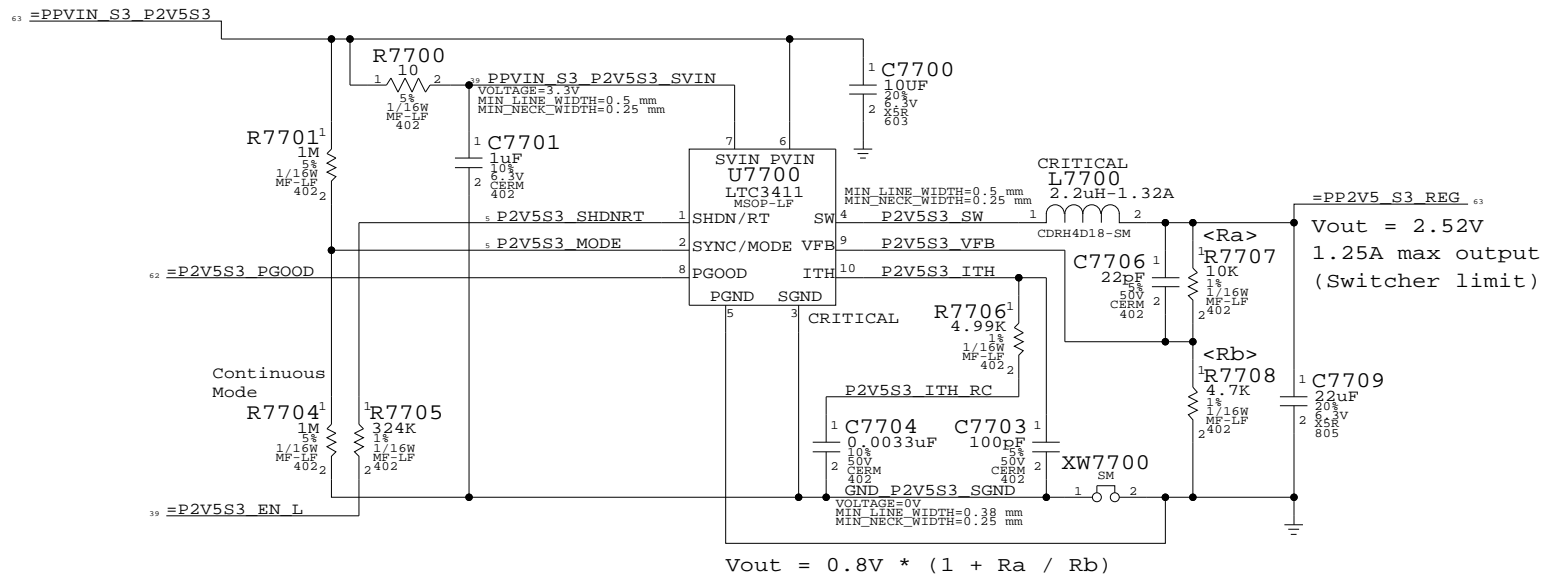
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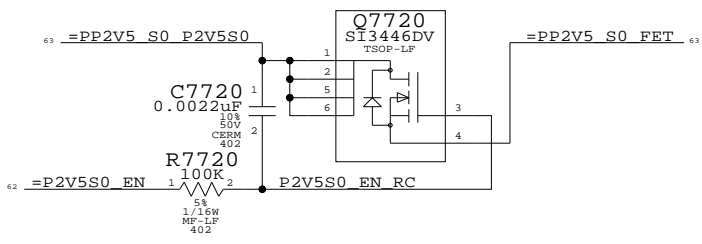
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	A
SCALE		SHT	OF
NONE		67	104

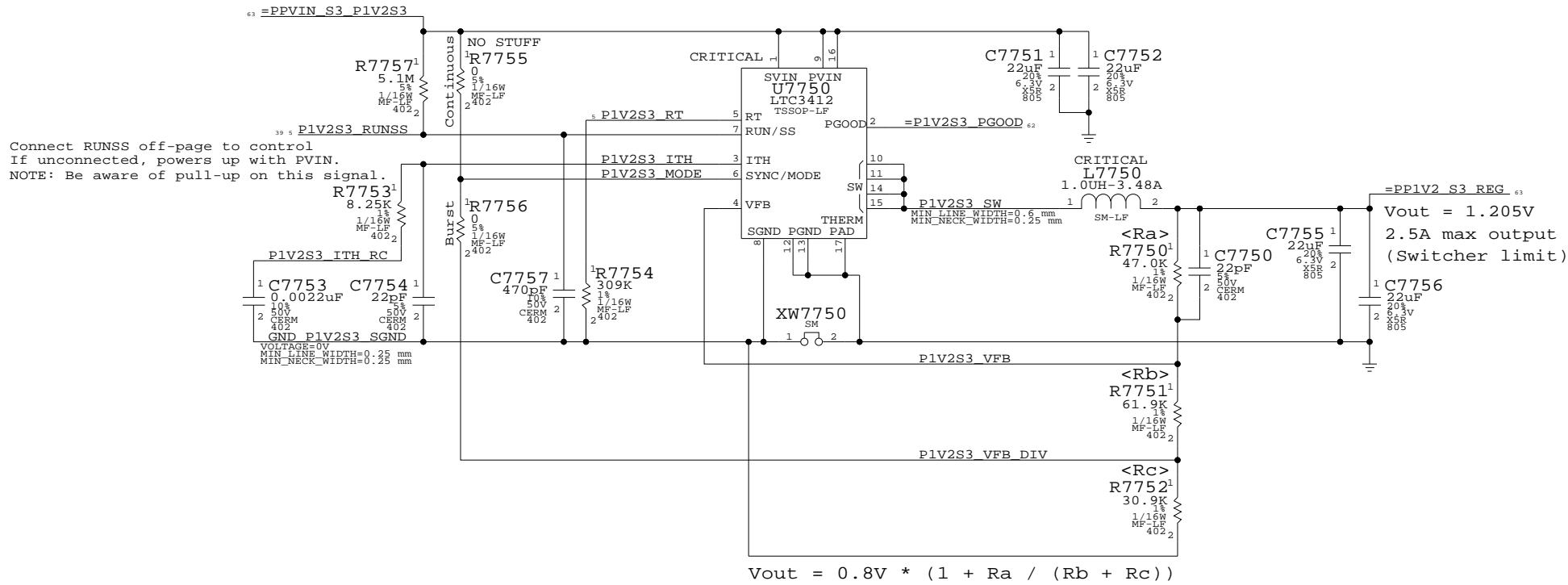
2.5V S3 Regulator



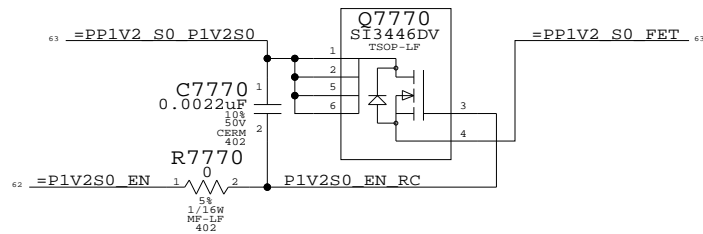
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



2.5V & 1.2V Regulators

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

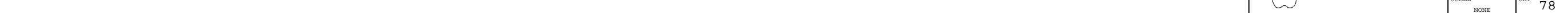
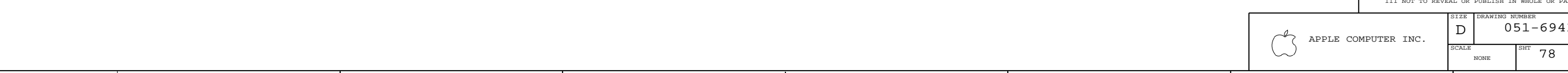
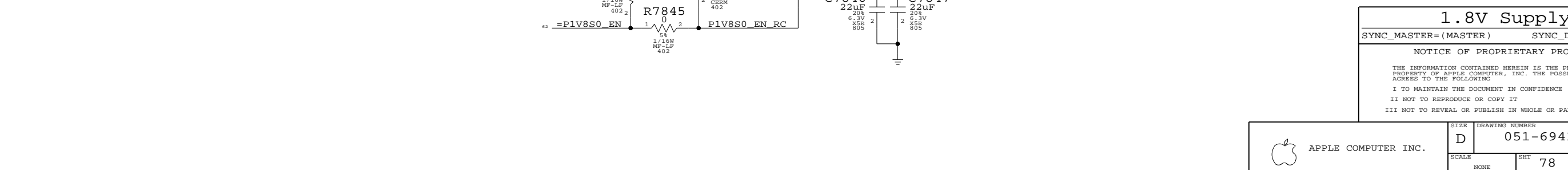
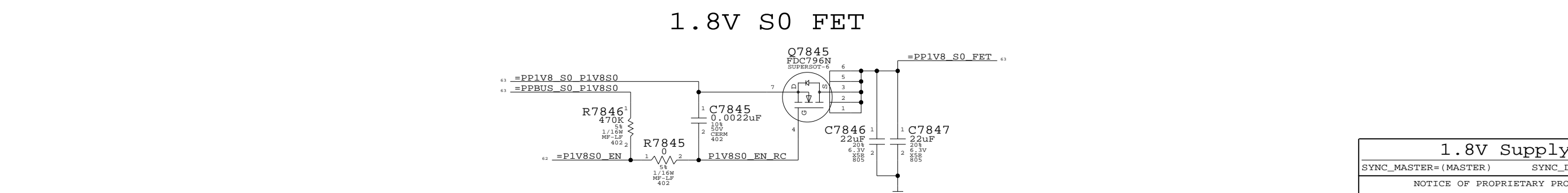
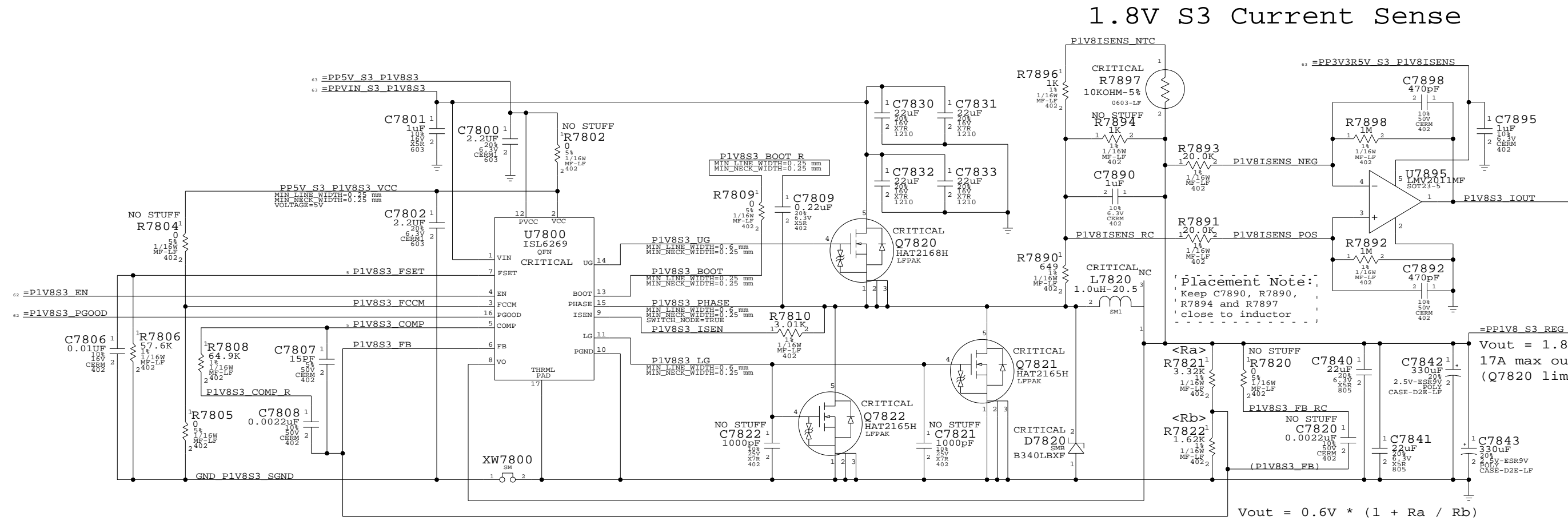
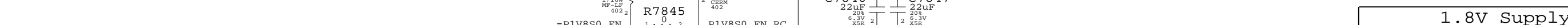
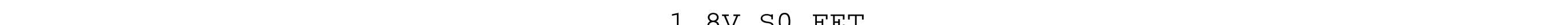
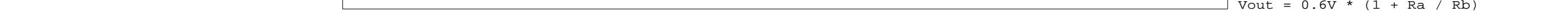
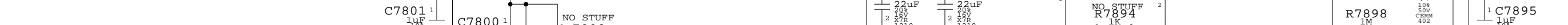
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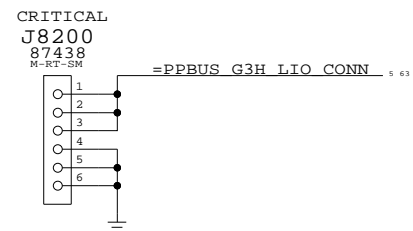
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II NOT TO REPRODUCE OR COPY IT

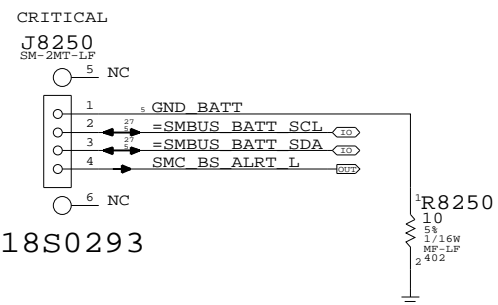
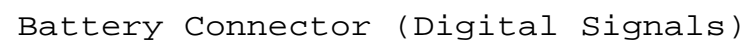
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518S0368



518S0293

PBus-In & Battery Connectors	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

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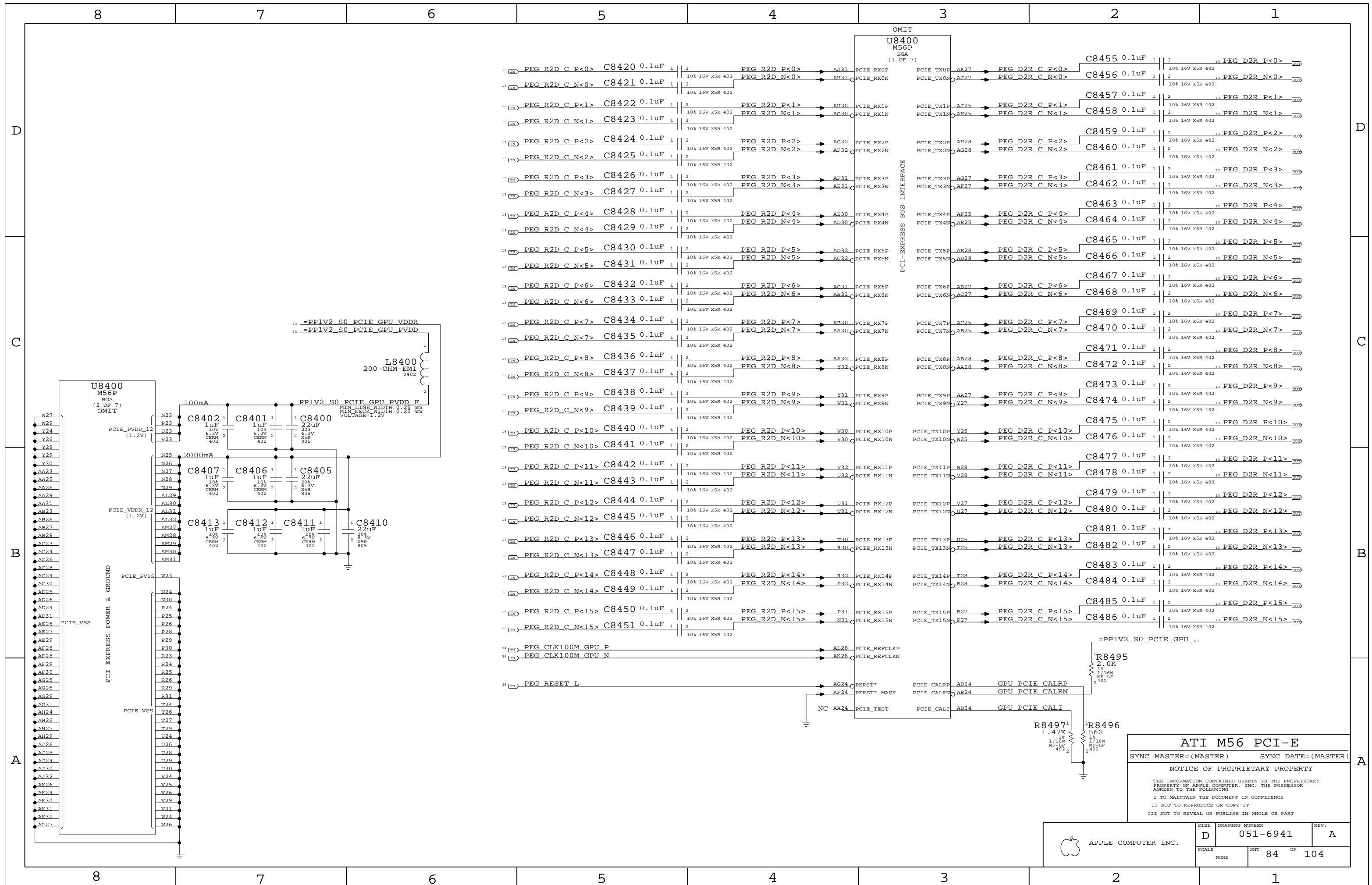
II NOT TO REPRODUCE OR COPY IT

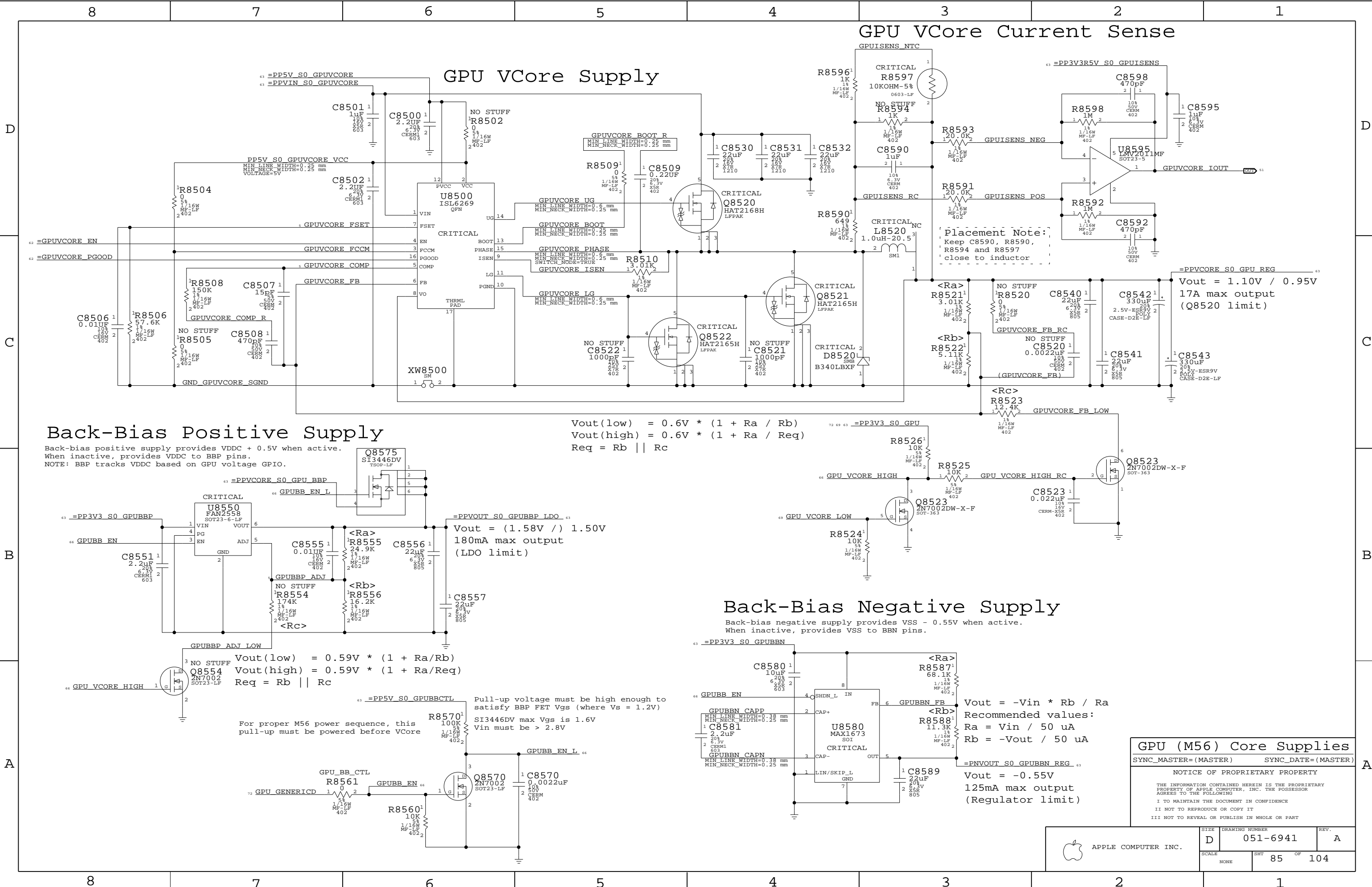
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APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-6941	REV. A
SCALE NONE	SHT 82	OF 104





GPU VCore Supply

GPU VCore Current Sense

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active. When inactive, provides VDDC to BBP pins.

NOTE: BBP tracks VDDC based on GPU voltage GPIO.

$$V_{out}(low) = 0.6V * (1 + R_a / R_b)$$
$$V_{out}(high) = 0.6V * (1 + R_a / R_{eq})$$
$$R_{eq} = R_b || R_c$$

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active. When inactive, provides VSS to BBN pins.

$$V_{out} = -V_{in} * R_b / R_a$$

Recommended values:
 $R_a = V_{in} / 50 \mu A$
 $R_b = -V_{out} / 50 \mu A$

$$V_{out} = -0.55V$$

125mA max output
(Regulator limit)

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE D DRAWING NUMBER 051-6941 REV. A

SCALE NONE SHT 85 OF 104

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

87654321

D

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B

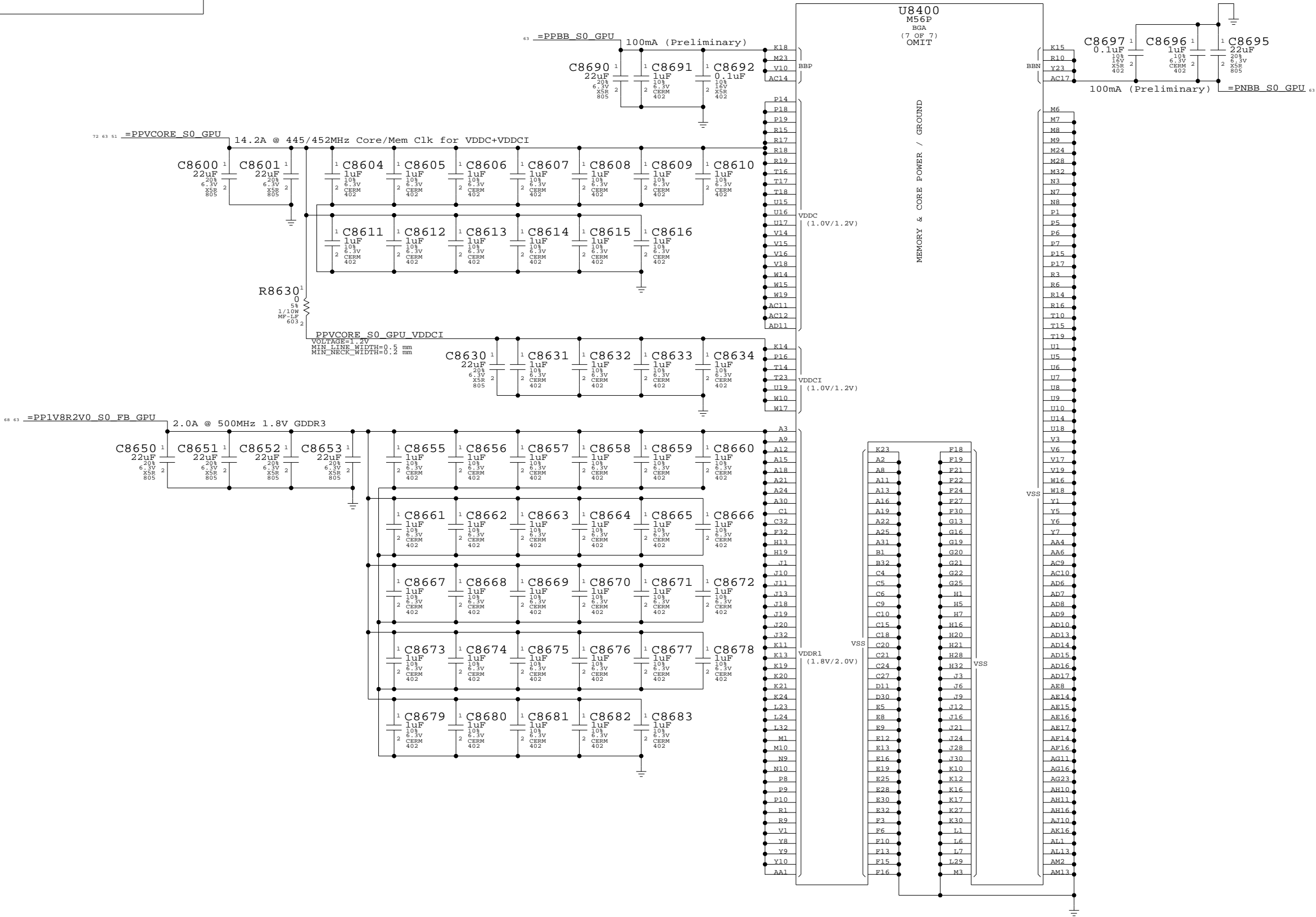
A

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ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-6941	A
SCALE		SHT	OF
NONE		86	104

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Page Notes

Power aliases required by this page:

- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

OMIT

U8400
M56P
BGA
(3 OF 7)

MEMORY INTERFACE A

READ STROBE

WRITE STROBE

CLKA0

CLKA0*

CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

CSA1_1*

CKEA1

RASA1*

CASA1*

WEA1*

ODTA1

CLKA0

CLKA0*

CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

CSA1_1*

CKEA1

RASA1*

CASA1*

WEA1*

ODTA1

CLKA0

CLKA0*

CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

CSA1_1*

CKEA1

RASA1*

CASA1*

WEA1*

ODTA1

CLKA0

CLKA0*

CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

CSA1_1*

CKEA1

RASA1*

CASA1*

WEA1*

ODTA1

CLKA0

CLKA0*

CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

CSA1_1*

CKEA1

RASA1*

CASA1*

WEA1*

ODTA1

CLKA0

CLKA0*

CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

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RASA1*

CASA1*

WEA1*

ODTA1

CLKA0

CLKA0*

CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

CSA1_1*

CKEA1

RASA1*

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CKEA1

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RASA0*

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WEA0*

ODTA0

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CLKA1*

CSA1_0*

CSA1_1*

CKEA1

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CASA1*

WEA1*

ODTA1

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CLKA0*

CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

CSA1_1*

CKEA1

RASA1*

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WEA1*

ODTA1

CLKA0

CLKA0*

CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

CSA1_1*

CKEA1

RASA1*

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CSA0_0*

CSA0_1*

CKEA0

RASA0*

CASA0*

WEA0*

ODTA0

CLKA1

CLKA1*

CSA1_0*

CSA1_1*

CKEA1

RASA1*

CASA1*

WEA1*

ODTA1

CLKA0

CLKA0*

CSA0_0*

CSA0_1*

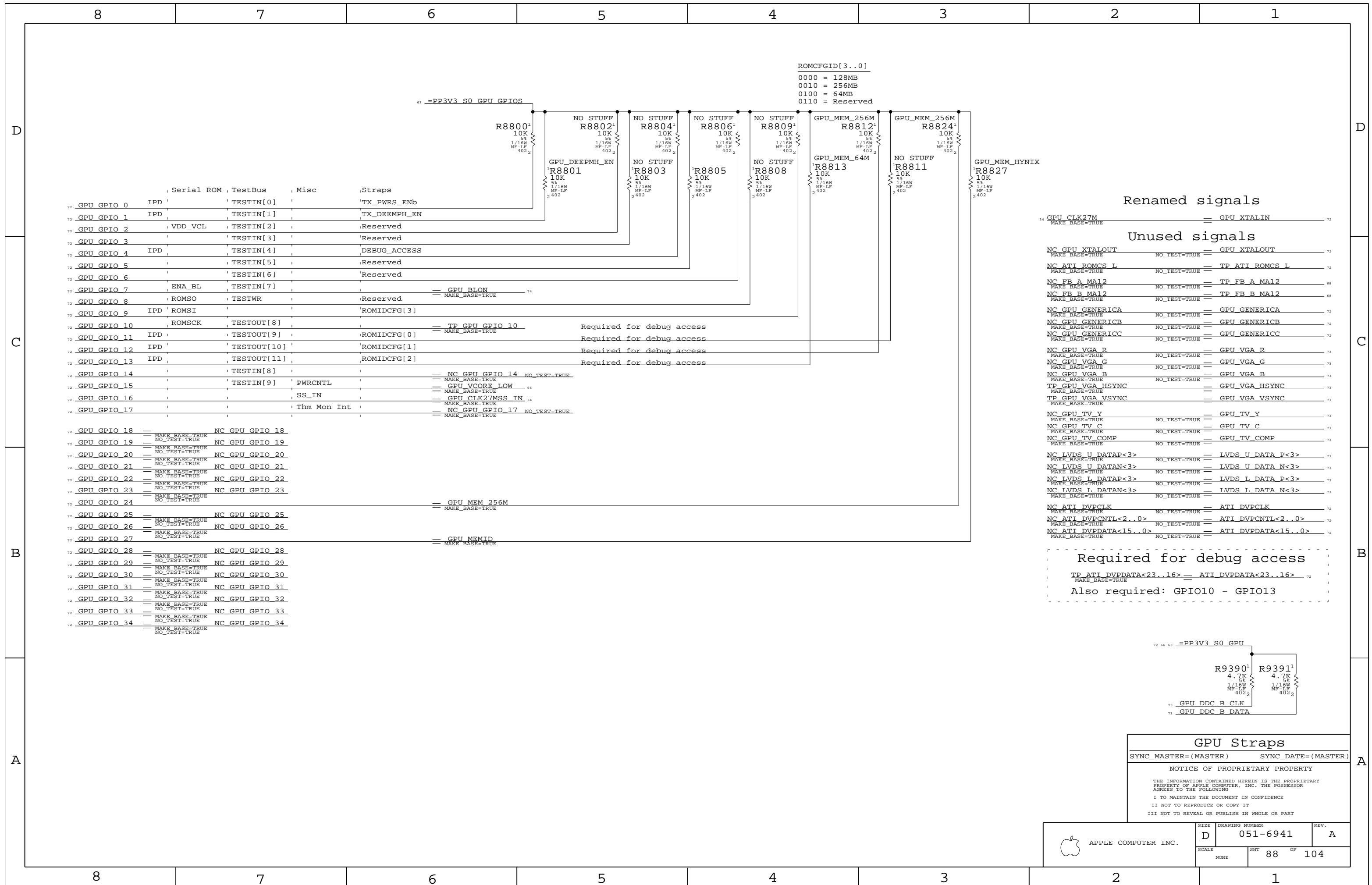
CKEA0

RASA0*

CASA0*

WEA0*

ODTA0



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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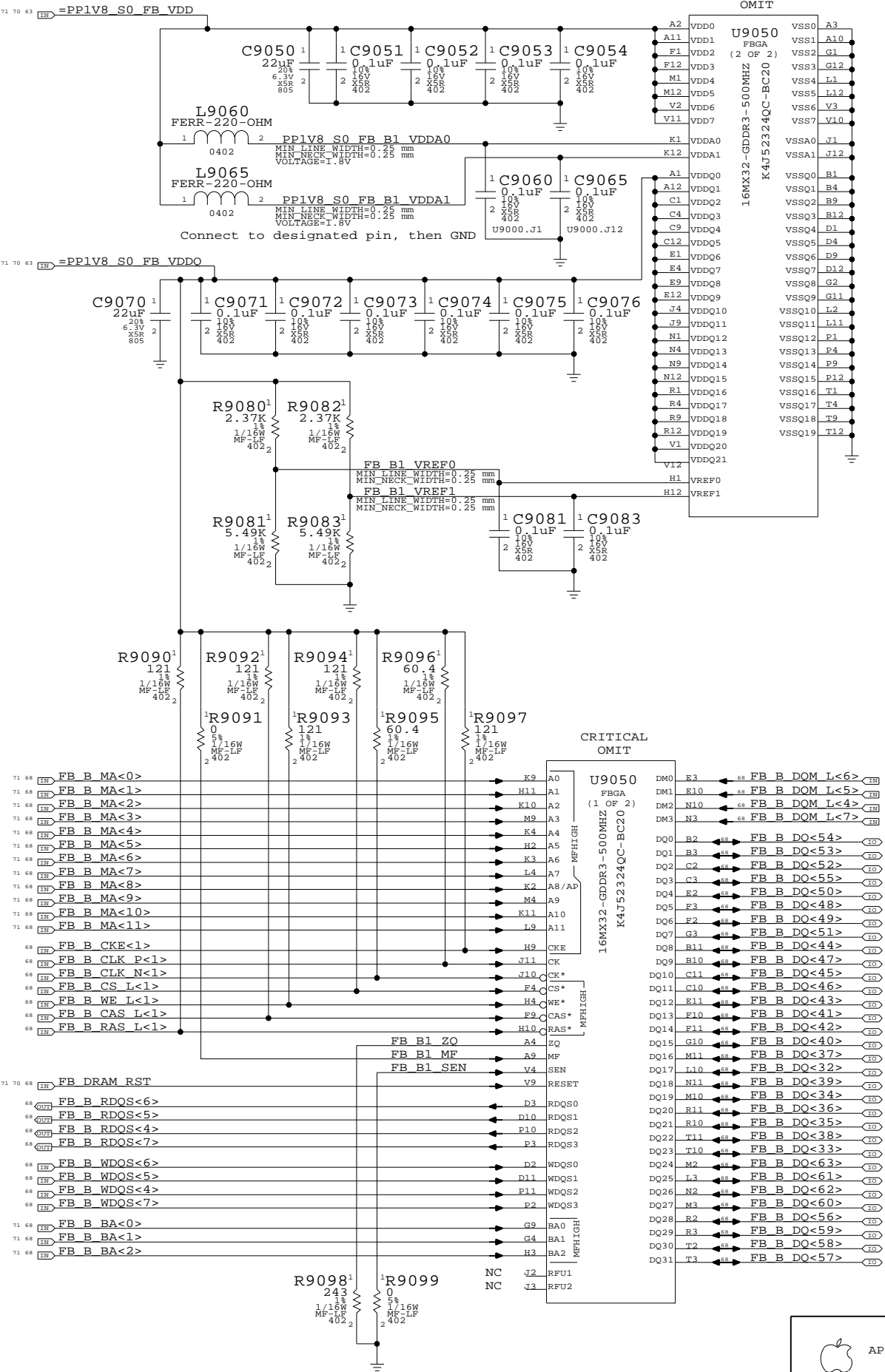
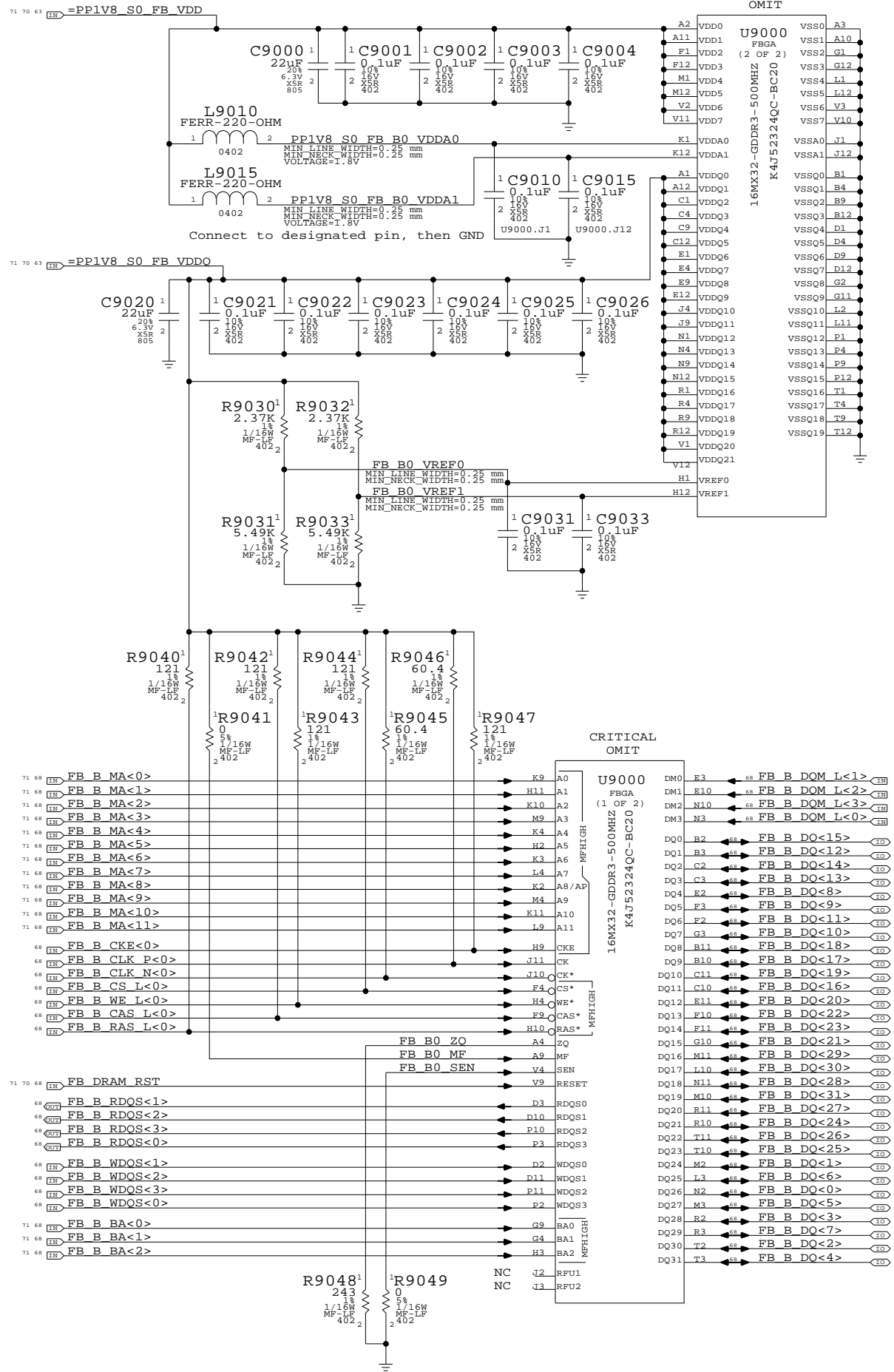
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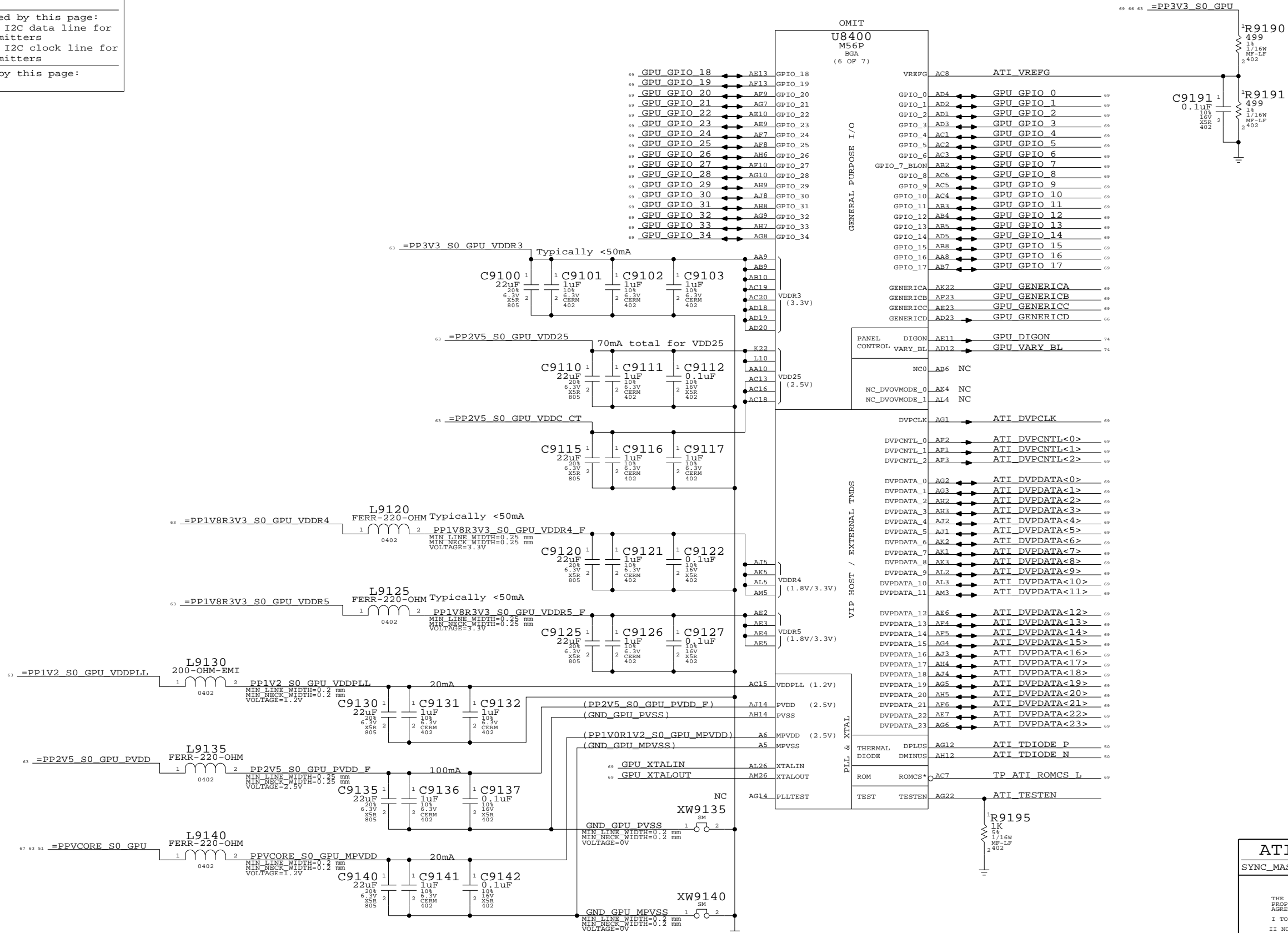
SIZE	DRAWING NUMBER	REV.
D	051-6941	A
SCALE	SHT	OF
NONE	90	104



[illegible]

```
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL
```

```
- =I2C_GPU_TMDS_SDA - I2C data line for
  external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for
  external TMDS transmitters
```

BOM op
(NONE)

U8400 M56P BGA (6 OF 7)		GENERAL PURPOSE I/O		VIP HOST / EXTERNAL TWDS		PLL & XTAL	
GPIO_18	VREFG	AC8	ATI VREFG				
GPIO_19							
GPIO_20	GPIO_0	AD4	GPU GPIO 0				
GPIO_21	GPIO_1	AD2	GPU GPIO 1				
GPIO_22	GPIO_2	AD1	GPU GPIO 2				
GPIO_23	GPIO_3	AD3	GPU GPIO 3				
GPIO_24	GPIO_4	AC1	GPU GPIO 4				
GPIO_25	GPIO_5	AC2	GPU GPIO 5				
GPIO_26	GPIO_6	AC3	GPU GPIO 6				
GPIO_27	GPIO_7_BLON	AB2	GPU GPIO 7				
GPIO_28	GPIO_8	AC6	GPU GPIO 8				
GPIO_29	GPIO_9	AC5	GPU GPIO 9				
GPIO_30	GPIO_10	AC4	GPU GPIO 10				
GPIO_31	GPIO_11	AB1	GPU GPIO 11				
GPIO_32	GPIO_12	AB4	GPU GPIO 12				
GPIO_33	GPIO_13	AB5	GPU GPIO 13				
GPIO_34	GPIO_14	AD5	GPU GPIO 14				
	GPIO_15	AD6	GPU GPIO 15				
	GPIO_16	AB8	GPU GPIO 16				
	GPIO_17	AB7	GPU GPIO 17				
VDDR3 (3.3V)	GENERIC A	AK22	GPU GENERIC A				
	GENERIC B	AE23	GPU GENERIC B				
	GENERIC C	AE23	GPU GENERIC C				
	GENERIC D	AD23	GPU GENERIC D				
	PANEL CONTROL	DIGON VARY_BL	AE11	GPU DIGON			
			AD12	GPU VARY BL			
VDD25 (2.5V)		NC0	AB6	NC			
	NC_DVOVMODE_0	AK4	NC				
	NC_DVOVMODE_1	AL4	NC				
	DVPCLK	AG1	ATI DVPCLK				
	DVP_CNTL_0	AE2	ATI DVP_CNTL<0>				
	DVP_CNTL_1	AF1	ATI DVP_CNTL<1>				
	DVP_CNTL_2	AF3	ATI DVP_CNTL<2>				
	DVPDATA_0	AG2	ATI DVPDATA<0>				
	DVPDATA_1	AG3	ATI DVPDATA<1>				
	DVPDATA_2	AH2	ATI DVPDATA<2>				
	DVPDATA_3	AH3	ATI DVPDATA<3>				
	DVPDATA_4	AJ2	ATI DVPDATA<4>				
	DVPDATA_5	AJ1	ATI DVPDATA<5>				
	DVPDATA_6	AK2	ATI DVPDATA<6>				
	DVPDATA_7	AK1	ATI DVPDATA<7>				
	DVPDATA_8	AK1	ATI DVPDATA<8>				
	DVPDATA_9	AL2	ATI DVPDATA<9>				
VDDR4 (1.8V/3.3V)	DVPDATA_10	AL3	ATI DVPDATA<10>				
	DVPDATA_11	AM3	ATI DVPDATA<11>				
	DVPDATA_12	AE6	ATI DVPDATA<12>				
	DVPDATA_13	AF4	ATI DVPDATA<13>				
	DVPDATA_14	AF5	ATI DVPDATA<14>				
	DVPDATA_15	AG4	ATI DVPDATA<15>				
	DVPDATA_16	AJ3	ATI DVPDATA<16>				
	DVPDATA_17	AH4	ATI DVPDATA<17>				
	DVPDATA_18	AH4	ATI DVPDATA<18>				
	DVPDATA_19	AG5	ATI DVPDATA<19>				
VDDPLL (1.2V)	DVPDATA_20	AH5	ATI DVPDATA<20>				
PVDD (2.5V)	DVPDATA_21	AE6	ATI DVPDATA<21>				
PVSS	DVPDATA_22	AE7	ATI DVPDATA<22>				
MPVDD (2.5V)	DVPDATA_23	AG6	ATI DVPDATA<23>				
MPVSS	THERMAL DIODE	DPLUS DMINUS	AG12 AH12	ATI TDIODE P ATI TDIODE N			
XTALIN	ROM	ROMCS*	AC7	TP ATI ROMCS L			
XTALOUT	TEST	TESTEN	AG22	ATI TESTEN			
PL1/TEST							

```

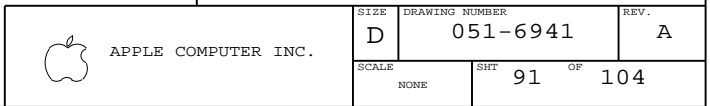
ATI M56 GPIO/DVO/Misc
-----
SYNC_MASTER=(MASTER)          SYNC_DATE=(MASTER)

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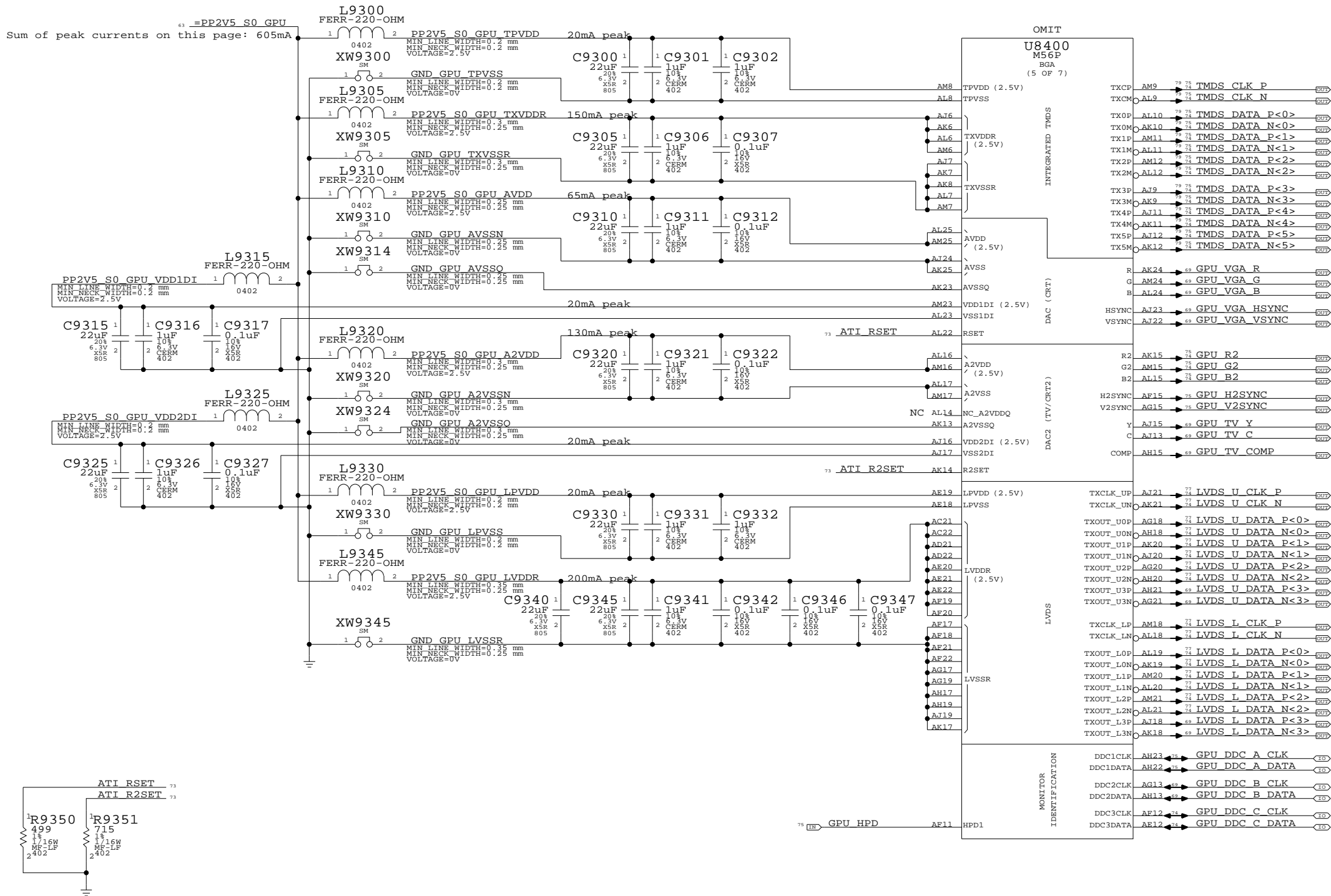
Power aliases required by this page:

- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents on this page: 605mA



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

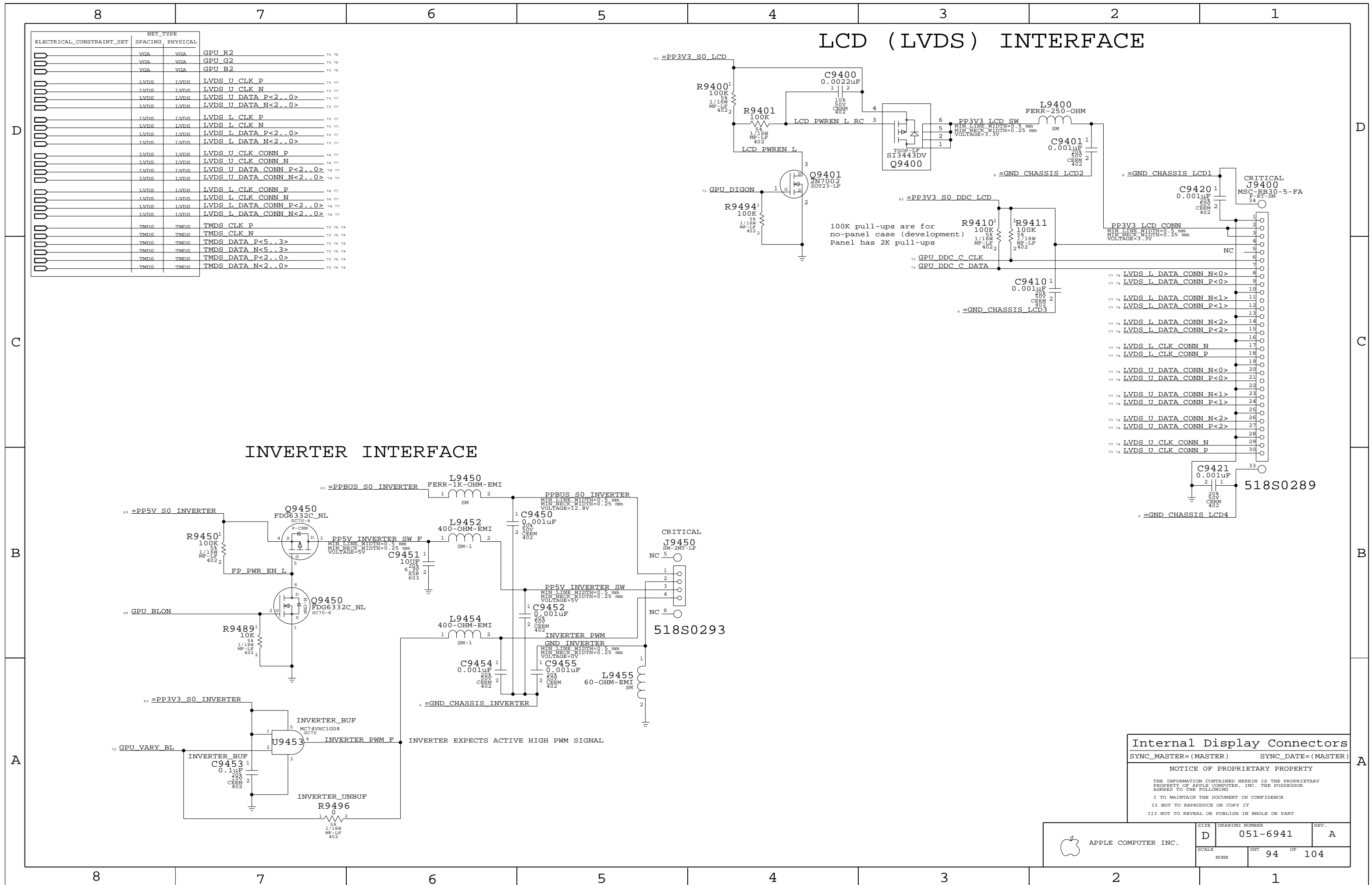
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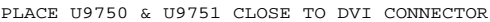
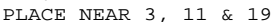
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	A
SCALE	SHT	OF
NONE	93	104



D

C

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)D

C



A

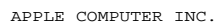
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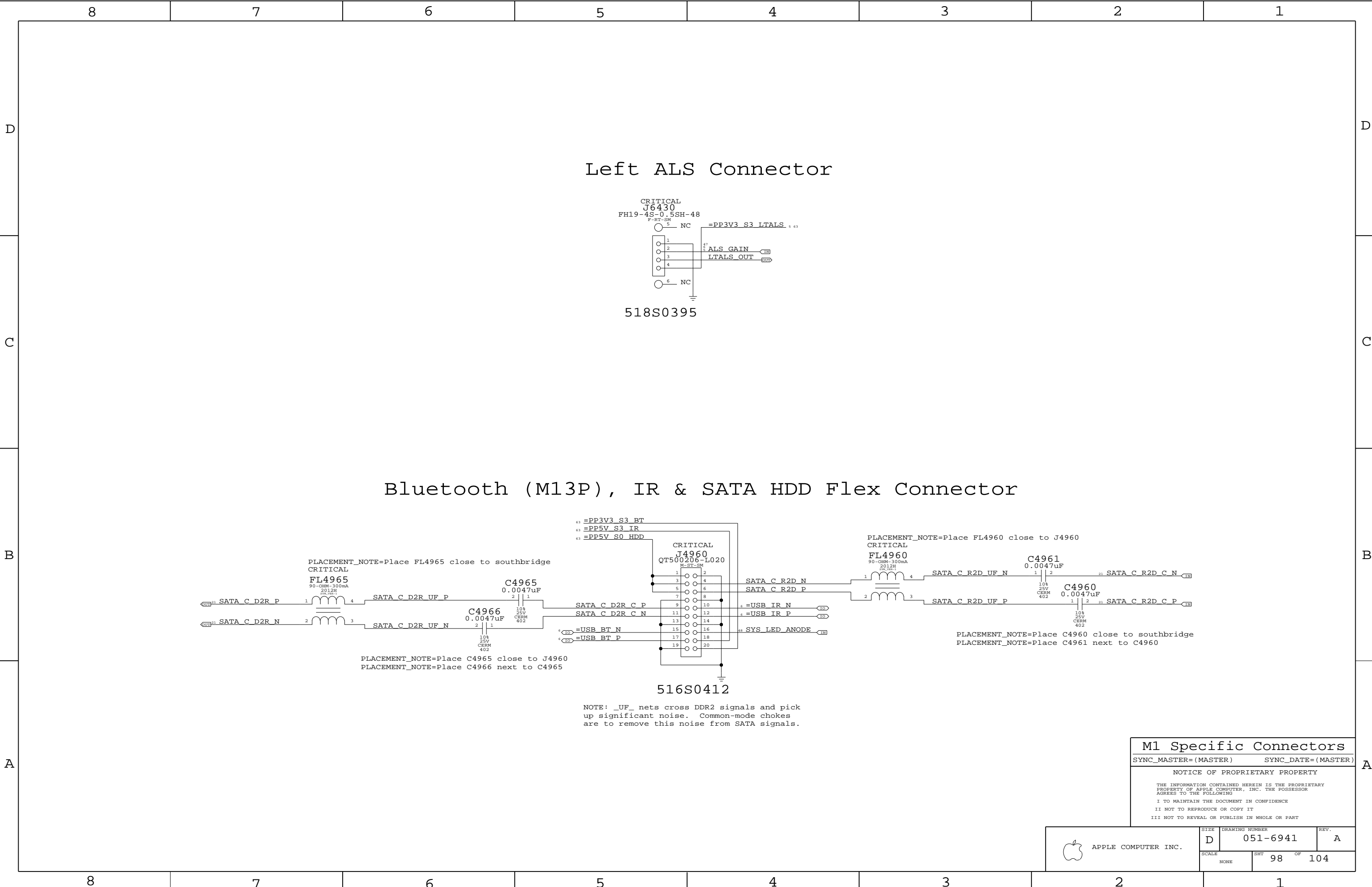
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SIZE D	DRAWING NUMBER 051-6941	REV. A
SCALE NONE	SHT 97	OF 104



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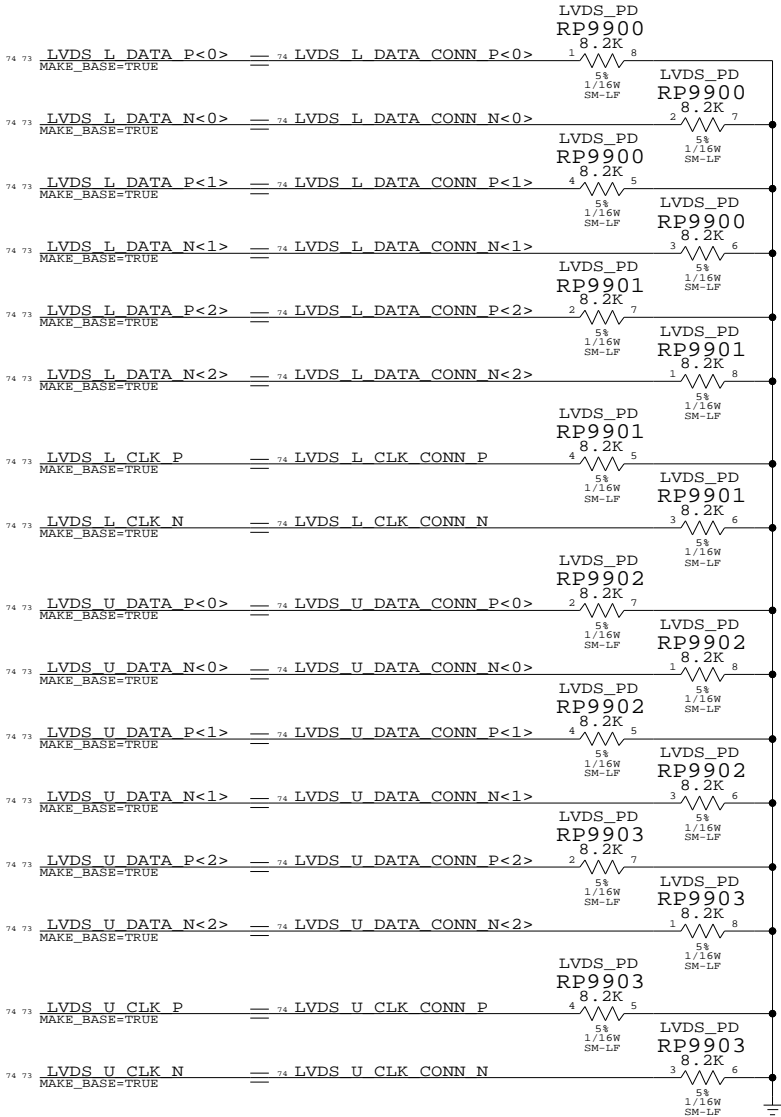
C

B

A

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs

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